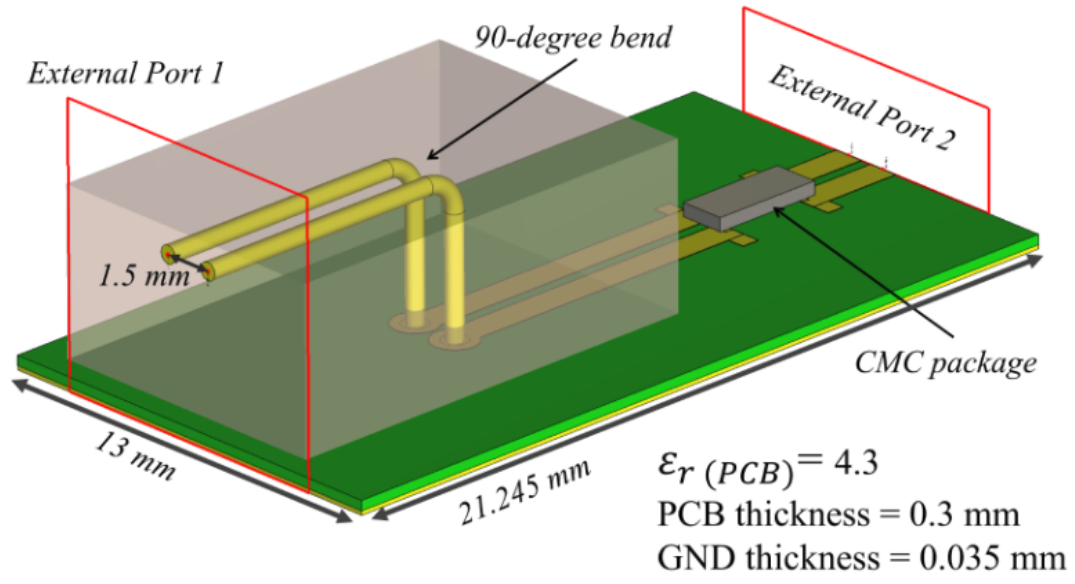


CP-1: Connector to CMC Package Interconnect

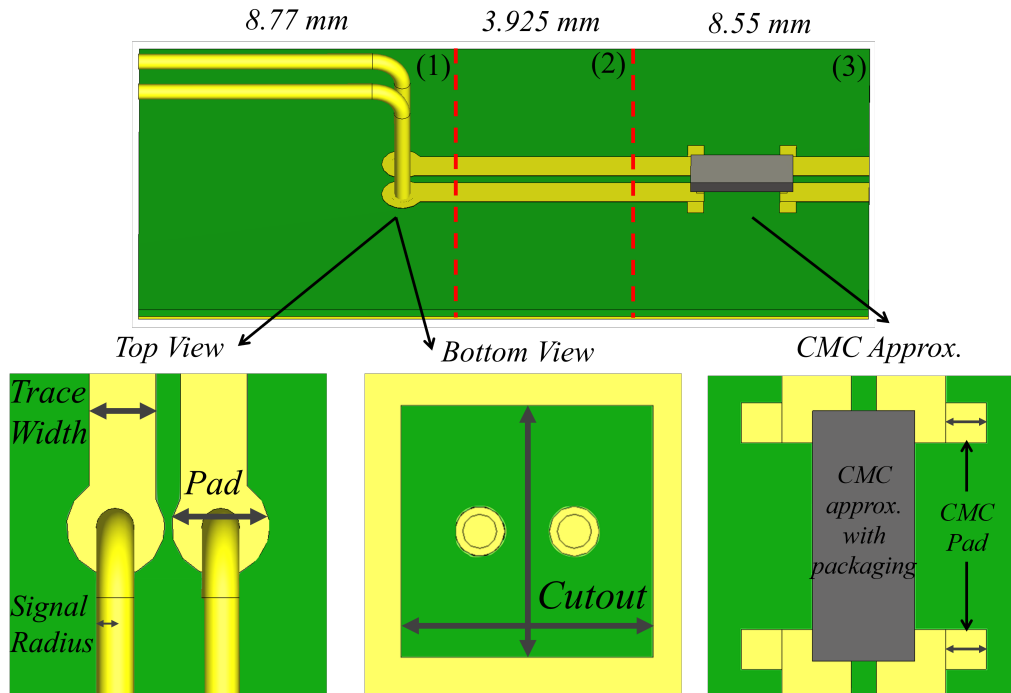
EMC/EMI Database

Institut für Theoretische Elektrotechnik
Hamburg University of Technology (TUHH)

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a)



b)

Figure 1: a) Parameterized 3D model of the complete interconnect (board size 13 mm $\times$ 21.245 mm, PCB thickness 0.3 mm, $\epsilon_r = 4.3$). b) Top view of the segmentation into the three sub-domains (1) input + 90° bend, (2) trace and (3) CMC approximation, with the definition of the varied geometry parameters.

1 Introduction

This dataset contains the full-wave simulated scattering parameters of a high-speed differential signal transition from a connector onto a printed circuit board (PCB), followed by a common-mode choke (CMC) in a surface-mount package. The structure and the simulations are described in [1]. You can find all information regarding the structure and the setup in the following chapters.

The structure is described by the board and stackup (materials, thicknesses), the connector with the 90-degree bend, the microstrip transmission lines, and the CMC approximation with packaging. The structure is evaluated as a whole and, following the segmentation described in [1], as three separate sub-domains. Further information is found in Section 3.

1.1 How to Cite?

If you use the provided data, cite both the dataset paper and the database paper [1, 2]:

M. Kvizhinadze, N. Talibzade, C. Yang, M. Mnich, and C. Schuster, “Optimization of Modal Reflection Parameters of PCB Connector and Common-Mode Choke Using Gaussian Process Regression and Segmentation,” in *2026 International Symposium on Electromagnetic Compatibility – EMC Europe*, Prague, Czech Republic, 2026.

M. Schierholz, A. Sanchez-Masis, A. Carmona-Cruz, X. Duan, K. Roy, C. Yang, R. Rimolo-Donadio, and C. Schuster, “SI/PI-Database of PCB-Based Interconnects for Machine Learning Applications,” in *IEEE Access*, vol. 9, pp. 34 423–34 432, Feb. 2021.

1.2 License

This and other EMC/EMI Databases may be used under the terms stated in the separate license agreement.

1.3 Data Structure

Included in the download are multiple files and folders, see Table 1. The four sub-datasets are summarized in Table 2. See Fig. 1 for the parameter definitions.

Table 1: Data Directory

Name	Type	Description
ReadMe.pdf	PDF-Document	This description
INPUT.BEND/	Directory	Sub-domain (1): input + 90° bend
TRACE/	Directory	Sub-domain (2): trace
CMC/	Directory	Sub-domain (3): CMC approximation
FULL/	Directory	Whole structure
parameter.csv	CSV Document (Delimiter = ',')	Parameter file of the sub-dataset with all parameter variations, see Section 3. One file in each sub-dataset directory.
variation/	Directory	EM simulation results (S-parameters) of the sub-dataset, see Section 4. One directory in each sub-dataset directory.

Table 2: Sub-datasets. LHS: Latin Hypercube Sampling, BO: Bayesian optimization, see Section 3.2.

Directory	Sub-domain	N_{Sam} (LHS + BO)	Varied parameters
INPUT_BEND/	(1) Input + 90° bend	30 (20 + 10)	R_SIG, L_CUT, W_CUT, R_PAD, W_TR, T_TR
TRACE/	(2) Trace	28 (20 + 8)	W_TR, T_TR
CMC/	(3) CMC approximation	40 (20 + 20)	W_TAP, W_TR, T_TR, L, K
FULL/	Whole structure	30 (20 + 10)	R_SIG, L_CUT, W_CUT, R_PAD, W_TAP, W_TR, T_TR, L, K
Total		128	

2 Structure

The structure comprises a differential pair of 90-degree angled input tubes mounted on a PCB, serving as a signal launch site, see Fig. 1. The signal propagates through differential microstrip pair and is terminated by a CMC approximation with packaging. If a parameter (capitalised) instead of a numerical value is given, this parameter was changed during the EM simulations. Further information on the parameters is found in Section 3.

2.1 Board Size

The board has a rectangular shape of 13 mm $\times$ 21.245 mm, see Fig. 1 a). The pitch of the two signal tubes is 1.5 mm.

2.2 Stackup and Materials

The PCB consists of one dielectric layer on a ground plane. The differential microstrip traces are placed on top of the dielectric. The stackup and the materials are summarized in Table 3. All conductors are modeled as perfect electric conductors (PEC) and the PCB dielectric is lossless.

Table 3: Stackup and materials

Layer / Part	Material	ϵ_r	Thickness / Size
Differential microstrip traces	PEC	–	T_TR
PCB dielectric	FR-4 (loss free)	4.3	0.3 mm
Ground plane	PEC	–	0.035 mm
CMC package	Dielectric	4	0.41 mm $\times$ 1.40 mm $\times$ 3.43 mm (H $\times$ W $\times$ L)

2.3 Segmentation into Sub-Domains

Following [1], the structure is divided into three sub-domains, see Fig. 1 b):

1. **Input + 90° bend** (8.77 mm): the right-angle transition domain with the 90-degree bend and the first part of the PCB traces. The parameters R_SIG, L_CUT, W_CUT and R_PAD are local to this sub-domain.
2. **Trace** (3.925 mm): the differential microstrip transmission line.
3. **CMC approximation** (8.55 mm): the connection and transition to the CMC package approximation, parameterized by the CMC pad width W_TAP and the CMC model parameters L and K.

The trace dimensions W_TR and T_TR are shared across all three sub-domains. The whole structure (FULL) contains all three sub-domains.

2.4 CMC Approximation

The behavior of the CMC is approximated by two coupled inductors, see Fig. 2 a), to avoid the computational overhead of simulating a choke geometry. The mutual inductance is

$$M = k\sqrt{L_1L_2}. \quad (1)$$

With $L_1 = L_2 = L$, $M = kL$, where $k \in [0, 1]$ is the coupling coefficient. Both L (L) and k (K) are varied. Four lumped ports are placed at the CMC pins inside the 3D model, see Fig. 2 b). They are not excitation sources; they connect the pin pads to the coupled-inductor network in the circuit simulator. Parasitic effects such as winding self-capacitance or inter-winding capacitance are not included.

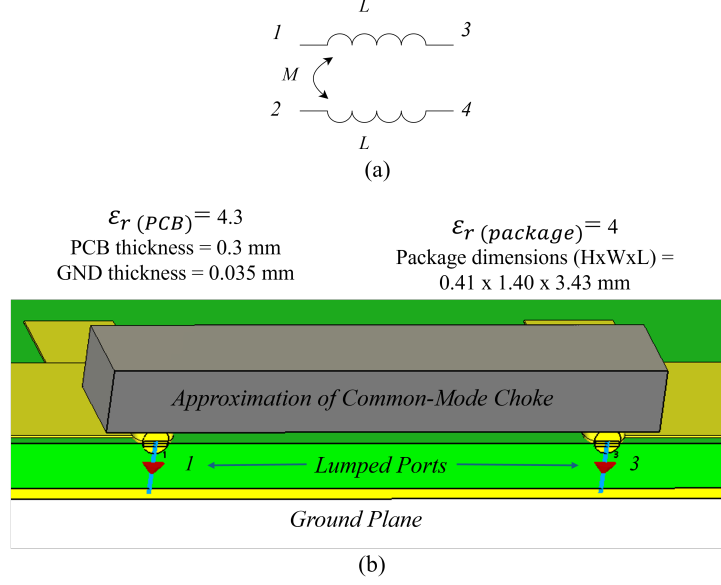


Figure 2: a) Equivalent circuit model of the CMC. b) 3D model used for the simulation of the CMC approximation with the lumped ports at the CMC pins.

3 Parameter Variation

Some parameters of the structure are varied throughout the EM simulations. Parameters are in general marked by capital letters. The design space is given in Table 4. The reference design of [1] is given for orientation. Each sub-dataset only contains the parameters of the sub-domains it includes, see Table 2.

Table 4: Design-space parameters and bounds

Parameter	Symbol	Name in parameter.csv	Range	Reference design
Signal tube radius (mm)	r_{sig}	R_SIG	[0.15, 0.43]	0.15
Cutout length (mm)	ℓ_{cut}	L_CUT	[2, 4]	4
Trace thickness (mm)	t_{tr}	T_TR	[0.015, 0.095]	0.015
Trace width (mm)	w_{tr}	W_TR	[0.1, 1]	0.55
Pad radius (mm)	r_{pad}	R_PAD	[0.1, 0.6]	0.6
Cutout width (mm)	w_{cut}	W_CUT	[1, 4]	4
CMC pad width (mm)	w_{tap}	W_TAP	[0.1, 1.2]	1
Coupling coefficient	k	K	[0.5, 1]	0.8
Inductance (nH)	L	L	[2, 10]	2
Relative permittivity (PCB)	ε_r	–	4.3 (fixed)	4.3
PCB thickness (mm)	t_{pcb}	–	0.3 (fixed)	0.3

3.1 Parameter Storage File <parameter.csv>

The file <parameter.csv> is a tabular file with multiple columns (Delimiter = ',') and rows. The first row has all the parameter names as named in Table 4. Each row is one EM simulation. The columns are:

- **SIMU_INDEX**: index of the simulation. The corresponding network parameters are found in the file <variation/SIMU_INDEX.s4p>.
- **SAMPLING**: LHS or BO, the method by which the sample was generated, see Section 3.2.
- One column per varied parameter of the sub-dataset, in the units of Table 4.

3.2 Sampling

The samples of each sub-dataset were generated as described in [1]. The first 20 samples (SIMU_INDEX 1–20) are an initial design obtained by Latin Hypercube Sampling (LHS). All following samples were proposed one after another by Bayesian optimization (BO) with a Gaussian process regression surrogate and the expected improvement acquisition function. The BO minimizes a scalar cost of the differential- and common-mode reflection parameters and stops by a custom early stopping rule. The SIMU_INDEX therefore follows the order of the evaluations.

4 EM-Simulation

The EM simulations were performed with CST Studio Suite 2025 [3] using the Finite Integration Technique (FIT) on a hexahedral mesh, with open boundary conditions. The frequency range is up to 20 GHz with 1001 linearly spaced frequency points.

4.1 Ports and Modes

The structure is excited by two waveguide ports located at the external interfaces of the structure, see Fig. 1 a). Each waveguide port carries two modes: mode 1 is the differential mode (DM) and mode 2 is the common mode (CM) with respect to the ground plane. For the sub-datasets, the waveguide ports are located at the boundaries of the respective sub-domain: port 1 on the input side and port 2 on the CMC side. For CMC and FULL, the 3D model was co-simulated with the coupled-inductor network of

Section 2.4 in the circuit simulator of CST, and only the external waveguide ports are contained in the results.

Every file <variation/SIMU_INDEX.s4p> is a 4-port Touchstone file (format GHz, S, magnitude/angle) with the port assignment of Table 5. All ports are referenced to $100\ \Omega$.

Table 5: Port assignment of the Touchstone files

Touchstone port	Waveguide port	Mode	Reference impedance
1	Port 1 (Connector side)	DM	$100\ \Omega$
2	Port 1 (Connector side)	CM	$25\ \Omega$
3	Port 2 (PCB side)	DM	$100\ \Omega$
4	Port 2 (PCB side)	CM	$25\ \Omega$

5 Acknowledgment

This project has received funding from the European Union’s EU Framework Programme for Research and Innovation Horizon Europe (Grant Agreement No. 101169295). Project website: pattern-dn.eu.

6 Contact

You can find the contact information and the person in charge at the Institut für Theoretische Elektrotechnik (TET), Hamburg University of Technology: <https://www.tet.tuhh.de/>

References

- [1] M. Kvizhinadze, N. Talibzade, C. Yang, M. Mnich, and C. Schuster, “Optimization of Modal Reflection Parameters of PCB Connector and Common-Mode Choke Using Gaussian Process Regression and Segmentation,” in *Proc. 2026 International Symposium on Electromagnetic Compatibility – EMC Europe*, Prague, Czech Republic, 2026.
- [2] M. Schierholz, A. Sanchez-Masis, A. Carmona-Cruz, X. Duan, K. Roy, C. Yang, R. Rimolo-Donadio, and C. Schuster, “SI/PI-Database of PCB-Based Interconnects for Machine Learning Applications,” *IEEE Access*, vol. 9, pp. 34 423–34 432, Feb. 2021.
- [3] Dassault Systèmes, CST Studio Suite, version 2025. [Online]. Available: www.3ds.com