14-Layer PCB with 9x8 Via Array using a Full Wave Simulation Tool

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SI/PI-Database

Institut für Theoretische Elektrotechnik

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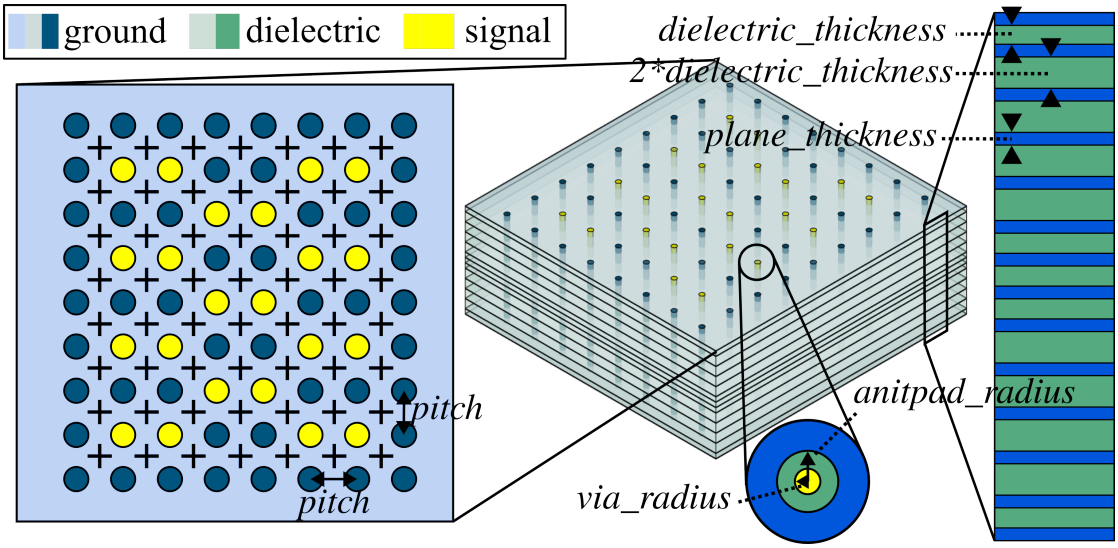

Figure 1: Overview of the printed circuit board (PCB) structure. The parameters are named as found in the data files.

1 Introduction

You can find all information regarding the printed circuit board (PCB) structure and setup in the following chapters. The PCB is described by the stackup, (order, type, material, thickness of layers) the board geometry (height, width), the via geometry (via radius, via antipad, etc.), the transmission lines (width, thickness, material) only if applicable and connectivity of vias, planes and transmissions lines.

Each of the previously mentioned aspects has an individual chapter. If instead of a numerical value a variable (italic letters) is given this parameter is varied during the electromagnetic (EM) simulations. Further information can be found in Section 3.

1.1 How to Cite?

If you use the provided data you have to reference by using at least the following Open Access paper [1] as well as the original publication of this dataset [2]:

M. Schierholz et al., "SI/PI-Database of PCB-Based Interconnects for Machine Learning Applications," in IEEE Access, vol. 9, pp. 34423-34432, 2021, doi: 10.1109/ACCESS.2021.3061788.

T.Hillebrecht et al., "Modeling and Improving Transmission of High-Speed Vias on PCBs up to 200 GHz," in 2026 IEEE 30th Workshop on Signal and Power Integrity (SPI), 2026, to be published.

1.2 License

Please be also aware of our license agreement. You can find further information in Section 5

1.3 Data Structure

Included in the download are multiple files and folders, See Table 1. See Fig. 1 for the parameter definitions.

1.4 Usage in Publications

This data set was used in the following publications:

- [2]

Table 1: Data Directory

Name	Type	Description
Description.pdf	PDF-Document	This Description
parameter.csv	CSV Document (Delimiter = ',')	Parameter file with all parameter variations, see Section 3.
variation/	Directory	Directory having all EM simulation results (S-Parameter), see Section 4

2 PCB Structure

The structure is a PCB with multiple planes, vias and materials. The vias and the stackup is explained in the following sections. If a parameter (italic font) instead of a numerical value is given this parameter was changed during the EM simulation. Further information of the parameters can be found in Section 3.

2.1 Board Size

The board has a rectangular shape, see Fig. 1. The dimensions are not important since a perfectly matched layer (PML) boundary condition is used for simulation.

2.2 Stackup

The structure has overall 13 dielectric cavities bounded at the top and bottom by metal planes. The planes are modeled as solid planes over the total size of the PCB. An overview of the stackup is shown in Table 2.

The connectivity of a layer is used to connect corresponding vias. Dielectric Material is not connected to any net. The Material definitions are shown in Table 3.

Table 2: Printed Circuit Board Stackup

Layer	**Type**	**Connectivity**	**Material**	**Thickness**
0	plane	GND	metal	*plane_thickness*
1	dielectric	None	dielmoat	*dielectric_thickness*
2	plane	GND	metal	*plane_thickness*
3	dielectric	None	dielmoat	2***dielectric_thickness*
4	plane	GND	metal	*plane_thickness*
5	dielectric	None	dielmoat	2***dielectric_thickness*
6	plane	GND	metal	*plane_thickness*
7	dielectric	None	dielmoat	2***dielectric_thickness*
8	plane	GND	metal	*plane_thickness*
9	dielectric	None	dielmoat	2***dielectric_thickness*
10	plane	GND	metal	*plane_thickness*
11	dielectric	None	dielmoat	*dielectric_thickness*
12	plane	GND	metal	*plane_thickness*
13	dielectric	None	dielmoat	*dielectric_thickness*
14	plane	GND	metal	*plane_thickness*
15	dielectric	None	dielmoat	*dielectric_thickness*
16	plane	GND	metal	*plane_thickness*
17	dielectric	None	dielmoat	2***dielectric_thickness*
18	plane	GND	metal	*plane_thickness*
19	dielectric	None	dielmoat	2***dielectric_thickness*
20	plane	GND	metal	*plane_thickness*
21	dielectric	None	dielmoat	2***dielectric_thickness*
22	plane	GND	metal	*plane_thickness*
23	dielectric	None	dielmoat	2***dielectric_thickness*
24	plane	GND	metal	*plane_thickness*
25	dielectric	None	dielmoat	*dielectric_thickness*
26	plane	GND	metal	*plane_thickness*

Table 3: Printed Circuit Board Material

Name	**metal**	**dielmoat**
Type	conductor	dielectric
Conductivity $\sigma\ \left(\frac{S}{m}\right)$	*conductivity*	not applicable
Rel. Permittivity ε_r	not applicable	*relative_permittivity*
Loss Tangent	not applicable	*loss_tangent*
Rel. Permeability μ_r	1.0	1.0

2.3 Via

The vias have multiple dimensional aspects, an overview is given in Fig. 2. The dielectric material (Dielectric) is the material from the dielectric layer, see Table 2. For each via array different via parameters are possible e.g. via radius.

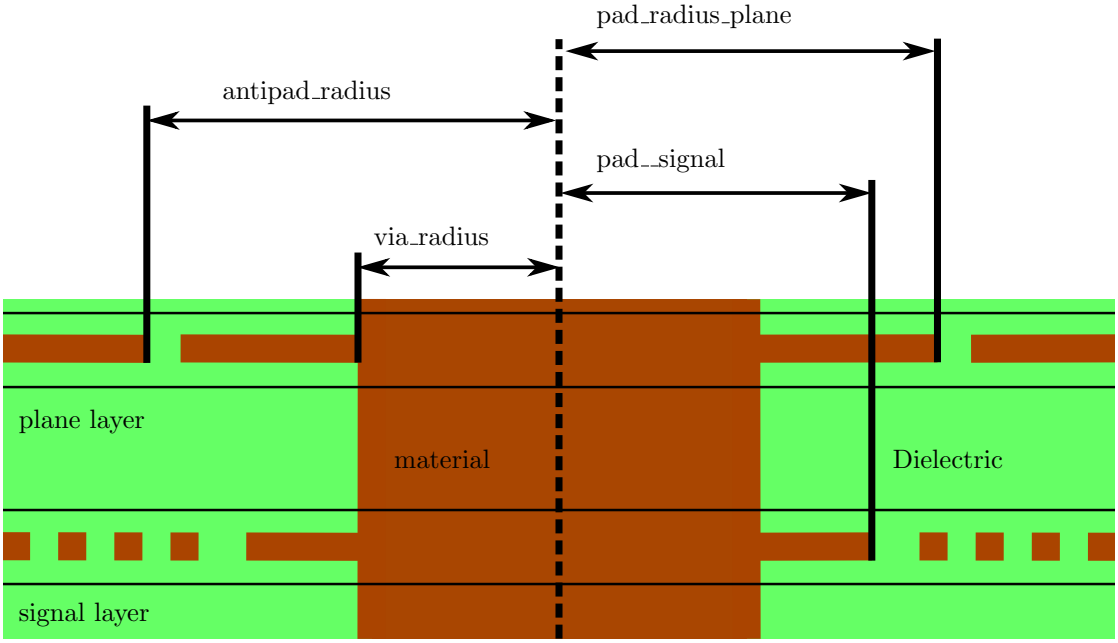

Figure 2: Overview of the via parameter e.g. via-radius. Pad radius signal and pad radius plane is relevant in the signal layer and plane layer respectively.

2.3.1 Via Model and Array

The vias of the array are organized in a 9x8 matrix with 22 signal vias and 50 ground vias, see Fig. 1. All ground vias are connected to all ground planes. The signal vias are arranged as differential pairs. In one simulation case additional ground vias are added as indicated by the crosses in Fig. 1

Table 4: Parameters Via Model: st_via

Parameter	**Value (mil)**
name	st_via
via_radius	*via_radius*
pad_radius_signal	0.0
antipad_radius	*antipad_radius*
pad_radius_plane	*pad_radius*
material	metal
cap_type	auto
cap_fd	no
cap_cfu	0.0
cap_cfl	0.0

3 Parameter Variation

Some parameters of the PCB are varied throughout the EM simulations. Parameters are in general marked by italic letters. All parameter variations are stored in the file **<parameter.csv>**, see Section 3.1.

3.1 Parameter Storage File <parameter.csv>

The file <parameter.csv> is a tabular file with multiple columns (Delimiter = ',') and rows. The first row has all the parameter names as named in the tables and figures of this document. Each row corresponds to a single EM simulation. By the column *simu_index* the corresponding network parameters can be found in the `variation` folder.

4 EM-Simulation

The EM simulations were performed with the FDTD solver of Feko © by Siemens Industry Software Inc. © [3]. The simulations are performed with PML boundary conditions. The frequency spectrum is 1 GHz to 200 GHz with 400 linearly spaced frequency points.

5 License agreement for usage of the SI/PI-Database

Institut für Theoretische Elektrotechnik, TUHH - December 2020

The SI/PI-Database is a collection of printed circuit board based structures which represent different electromagnetic aspects for signal integrity and power integrity applications. The structures have different components and interconnecting elements e.g. vias, via-arrays, power, ground planes. Each structure contains many variations with the according simulation results. All structures were simulated with a physics-based approach developed by TUHH.

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chine learning applications," IEEE Access, vol. 9, pp. 34 423–34 432, Feb. 2021

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6 Contact

You can find the contact information and the person in charge SI/PI-Database at TET: https://www.tet.tuhh.de/en/si-pi-database/

References

[1] M. Schierholz, A. Sanchez-Masis, A. Carmona-Cruz, X. Duan, K. Roy, C. Yang, R. Rimolo-Donadio, and C. Schuster, "SI/PI-Database of PCB-Based Interconnects for Machine Learning Applications," *IEEE Access*, vol. 9, pp. 34 423–34 432, Feb. 2021.

[2] T. Hillebrecht, J. Alfert, P. Lelekas, N. Sismanis, G. Bouzianas, and C. Schuster, "Modeling and Improving Transmission of High-Speed Vias on PCBs up to 200 GHz," in *2026 IEEE 30th Workshop on Signal and Power Integrity (SPI)*, to be published.

[3] Siemens Industry Software Inc.., *The FDTD solver in Simcenter Feko*. Troy, Michigan, U.S.: Siemens Industry Software Inc.. [Online]. Available: https://www.siemens.com/en-us/products/simcenter/electromagnetics-simulation/feko/