4-Layer Eurocard based PDN with medium via array

SI/PI-Database
Institut für Theoretische Elektrotechnik
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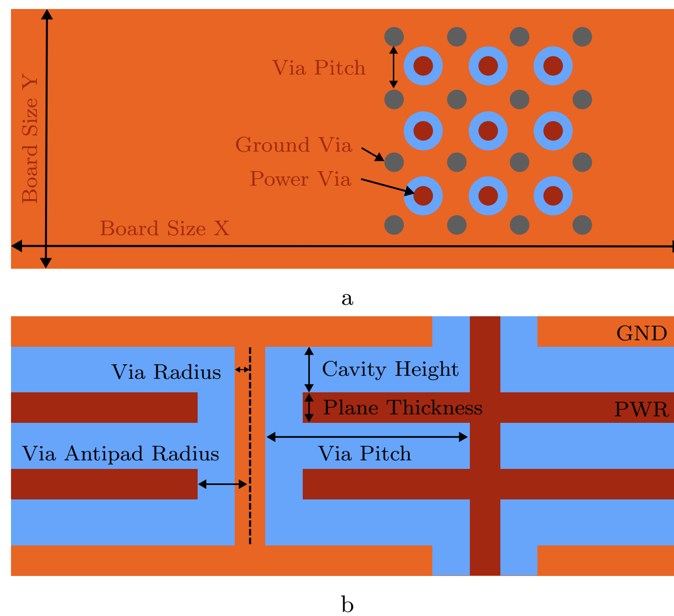


Figure 1: a) Top view of the printed circuit board (PCB), b) side view of the printed circuit board (PCB). The parameters are named as found in the data files. The via array consists of 9 power vias with interstitial ground vias. The vias have the same porperties as specified in the parameter.csv file, e.g. via radius.

1 Introduction

You can find all information regarding the printed circuit board (PCB) structure and setup in the following chapters. The PCB is described by the stackup, (order, type, material, thickness of layers) the board geometry (height, width), the via geometry (via radius, via antipad, etc.), the transmission lines (width, thickness, material) only if applicable and connectivity of vias, planes and [transmissions lines]. The PCB size is defined based on the eurocard standard and a medium via array is placed on the PCB.

Each of the previously mentioned aspects has an individual chapter. If instead of a numerical value a variable (capital letters) is given this parameter is varied during the electromagnetic (EM) simulations. Further information are found in Section 3.

1.1 How to Cite?

If you use the provided data you have to reference by using at least the following Open Access paper [1]:

> M. Schierholz et al., "SI/PI-Database of PCB-Based Interconnects for Machine Learning Applications," in IEEE Access, vol. 9, pp. 34423-34432, 2021, doi: 10.1109/ACCESS.2021.3061788.

This data set was used in the following publications:

> J. Hessling, H. Manoharan, N. Kharshiladze, C Hwang and C. Schuster, "Improvement of ML Based Fast Impedance Matrix Prediction for Subsequent PCB Decoupling" accepted for presentation at IEEE International Symposium on Electromagnetic Compatibility, Signal & Power Integrity (EMC+SIPI), 2026. [2]

1.2 License

Please be also aware of our license agreement. You can find further information in Section 5

1.3 Data Structure

Included in the download are multiple files and folders, See Table 1. See Fig. 1 for the parameter definitions.

Table 1: Data Directory

Name	Type	Description
ReadMe.pdf	PDF-Document	This Description
parameter.csv	CSV Document (Delimeter = ',')	Parameter file with all parameter variations, see Section 3.
variation/	Directory	Directory having all EM simulation results (S-Parameter), see Section 4

2 PCB Structure

The structure is a PCB with 3 cavities, 4 power vias and varying materials. The vias and the stackup are explained in the following sections. If a parameter (italic font) instead of a numerical value is given this parameter was changed during the EM simulation. Further information of the parameters are found in Section 3.

2.1 Board Size

The board has a rectangular shape based on the eurocard standard, see Fig. 1. The dimensions are 6300 mil and 3940 mil in X- and Y-direction respectively.

2.2 Stackup

The structure has overall 3 cavities with 4 planes, and 1 dielectric. The planes are modeled as solid planes over the total size of the PCB. An overview of the stackup is shown in Table 2.

The connectivity of a layer is used to connect corresponding vias. Dielectric Material is not connected to any net. The Material definitions are shown in Table 3.

Table 2: Printed Circuit Board Stackup

Layer	Type	Connectivity	Material	Thickness
0	plane	GND	copper	**1 mil**
1	dielectric	None	dielmoat	**[TDIEL]**
2	plane	PWR	copper	**1 mil**
3	dielectric	None	dielmoat	**[TDIEL]**
4	plane	PWR	copper	**1 mil**
5	dielectric	None	dielmoat	**[TDIEL]**
6	plane	GND	copper	**1 mil**

Table 3: Printed Circuit Board Material

Name	**copper**	**dielmoat**
Type	conductor	dielectric
Conductivity $\sigma\ \left(\frac{S}{m}\right)$	**5.8e7 S/m**	not applicable
Rel. Permittivity ε_r	not applicable	**[PERMITTIVITY]**
Loss Tangent	not applicable	**0.02**
Rel. Permeability μ_r	1.0	1.0

2.3 Via

The vias have multiple dimensional aspects, an overview is given in Fig. 2. The dielectric material (Dielectric) is the material from the dielectric layer, see Table 2. For each via array different via parameters are possible e.g. via radius. Additional information of the parameters can be found in the CONMLS user manual CONMLS by TET).

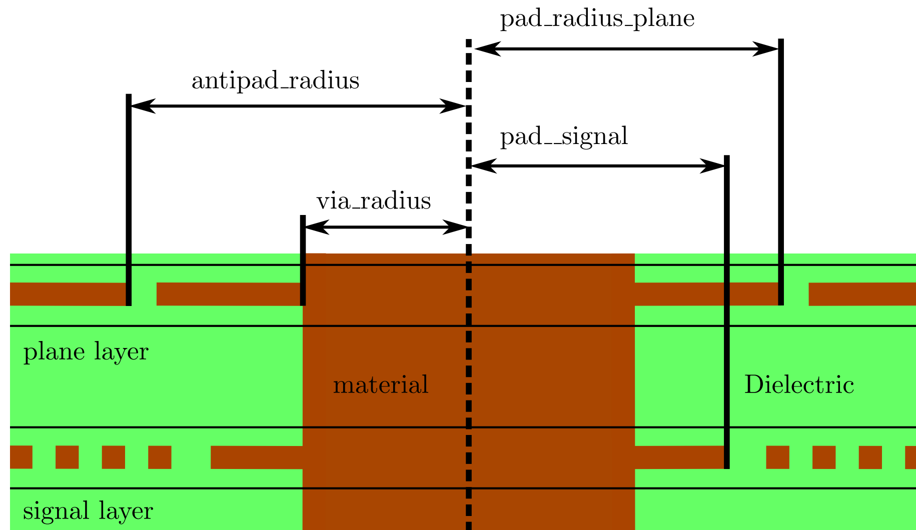


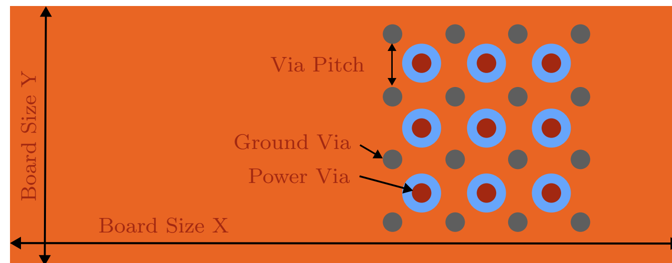
Figure 2: Overview of the via parameter e.g. via-radius. Pad radius signal and pad radius plane is relevant in the signal layer and plane layer respectively.

2.3.1 A1: Via Model and Array

The vias of array $A1$ are organized in a medium array with nine power vias in the center and interstitial ground vias, see Fig. 3. All ground vias are connected to all ground planes. All power vias are connected to all power planes. The pitch is defined according to Fig. 3.

Table 4: Parameters Via Model: a1_via_model

Parameter	**Value (mil)**
name	a1_via_model
via_radius	**[A1_VIARADIUS]**
inner_radius	0.0
pad_radius_signal	0.0
antipad_radius	**15**
pad_radius_plane	0.0
material	copper
cap_type	auto
cap_fd	no
cap_cfu	0.0
cap_cfl	0.0



a

Figure 3: Top view of $A1$ with 9 power vias and interstitial ground vias. All vias are connected to their respective reference planes.

3 Parameter Variation

Some parameters of the PCB are varied throughout the EM simulations. Parameters are in general marked by capital letters. All parameter variations are stored in the file **<parameter.csv>**, see Section 3.1.

3.1 Parameter Storage File <parameter.csv>

The file <parameter.csv>is a tabular file with multiple columns (Delimeter = ',') and rows. The first row has all the parameter names as named in the tables and figures of this document. Each row is one EM simulation. By the column SIMU_INDEX the corresponding network parameters are found in the variation/ folder.

4 EM-Simulation

The EM simulations are carried out with an in house developed simulation tool. The tool is based on physics based via models [3–5]. In recent work of the institute many correlations with full-wave solver have been made with a high accuracy.

The simulations are performed with perfect magnetic conducting (PMC) boundary conditions. The frequency spectrum is 1 MHz to 1 GHz with 121 logarithmically spaced frequency points.

5 License agreement for usage of the SI/PI-Database

Institut für Theoretische Elektrotechnik, TUHH - December 2020

The SI/PI-Database is a collection of printed circuit board based structures which represent different electromagnetic aspects for signal integrity and power integrity applications. The structures have different components and interconnecting elements e.g. vias, via-arrays, power, ground planes. Each structure contains many variations with the according simulation results. All structures were simulated with a physics-based approach developed by TUHH.

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6. When data from the SI/PI-Database is used the following reference has to be given: M. Schierholz, A. Sanchez-Masis, A. Carmona-Cruz, X. Duan, K. Roy, C. Yang, R. Rimolo-Donadio, and C. Schuster, "SI/PI-database of PCB

based interconnects for machine learning applications," IEEE Access, vol. 9, pp. 34 423–34 432, Feb. 2021

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6 Contact

You can find the contact information and the person in charge SI/PI-Database at TET: https://www.tet.tuhh.de/en/si-pi-database/

References

[1] M. Schierholz, A. Sanchez-Masis, A. Carmona-Cruz, X. Duan, K. Roy, C. Yang, R. Rimolo-Donadio, and C. Schuster, "SI/PI-Database of PCB-Based Interconnects for Machine Learning Applications," *IEEE Access*, vol. 9, pp. 34 423–34 432, Feb. 2021.

[2] J. Hessling, H. Manoharan, N. Kharshiladze, C. Hwang, and C. Schuster, "Improvement of ML Based Fast Impedance Matrix Prediction for Subsequent PCB Decoupling," in *accepted for presentation at 2026 IEEE International Symposium on Electromagnetic Compatibility, Signal & Power Integrity (EMC+SIPI).* Texas, USA: IEEE, 2026.

[3] R. Rimolo-Donadio, X. Gu, Y. Kwark, M. Ritter, B. Archambeault, F. de Paulis, Y. Zhang, J. Fan, H.-D. Brüns, and C. Schuster, "Physics-Based Via and Trace Models for Efficient Link Simulation on Multilayer Structures Up to 40 GHz," *IEEE Transactions Microwave Theory and Techniques*, vol. 57, no. 8, pp. 2072–2083, Aug. 2009.

[4] X. Duan, R. Rimolo-Donadio, H.-D. Brüns, and C. Schuster, "A Combined Method for Fast Analysis of Signal Propagation, Ground Noise, and Radiated Emission of Multilayer Printed Circuit Boards," *IEEE Transactions on Electromagnetic Compatibility*, vol. 52, no. 2, pp. 487–495, May 2010. [Online]. Available: https://doi.org/10.1109/temc.2010.2041238

[5] S. Müller, F. Happ, X. Duan, R. Rimolo-Donadio, H.-D. Bruns, and C. Schuster, "Complete Modeling of Large Via Constellations in Multilayer Printed Circuit Boards," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 3, no. 3, pp. 489–499, Mar. 2013. [Online]. Available: https://doi.org/10.1109/tcpmt.2012.2234211