Link on 11 Cavity PCB with two 10x10 Via-Arrays

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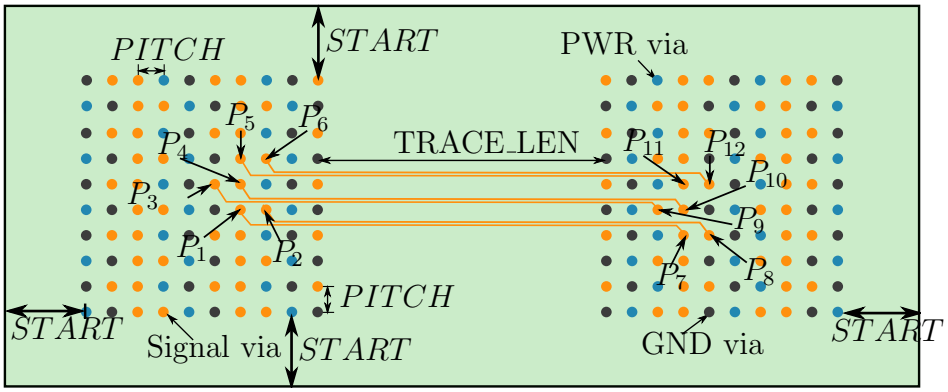

1 Introduction

You can find all information regarding the printed circuit board (PCB) structure and setup in the following chapters. The PCB is described by the stackup, (order, type, material, thickness of layers) the board geometry (height, width), the via geometry (via radius, via antipad, etc.), the transmission lines (width, thickness, material) only if applicable and connectivity of vias, planes and [transmissions lines].

Each of the previously mentioned aspects has an individual chapter. If instead of an numerical value a variable (capital letters) is given this parameter is varied during the electromagnetic (EM) simulations. Further information are found in Chap. 3.

This structure was previously used in publications from TET @ TUHH, see Chap. 1.2.

1.1 Data Structure

Included in the download are multiple files and folders, See Tab. 1. See Fig. 1 for the parameter definitions.

Table 1: Data Directory

Name	**Type**	**Description**
ReadMe.pdf	PDF-Document	This Description
parameter.csv	CSV Document (Delimeter = ',')	Parameter file with all parameter variations, see Chap. 3.
variation/	Directory	Directory having all EM simulation results (S-Parameter), see Chap 4

1.2 Appearance in TET Publications

The PCB structure was used in multiple publications. An excerpt is listed below.

- [1]
- [2]

2 PCB Structure

The structure is a PCB with multiple planes, vias and materials. The vias and the stackup is explained in the following sections. If a parameter (italic font) instead of a numerical value is given this parameter was changed during the EM simulation. Further information of the parameters are found in Chap. 3.

2.1 Board Size

The height and width of the PCB is listed in Tab. 2 .

Table 2: Printed Circuit Board Shape

Height (mil)	**Width (mil)**
$2 \cdot START + 9 \cdot PITCH$	$2 \cdot START + TRACE\_LEN + 18 \cdot PITCH$

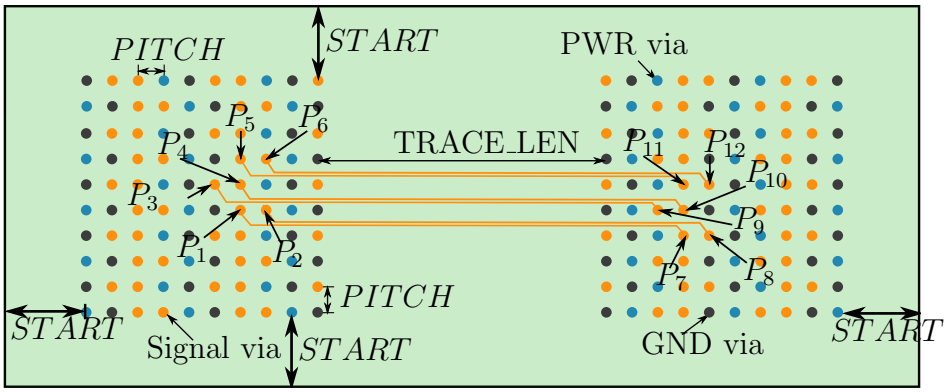

Figure 1: Top view of the PCB in the first signal layer. Orange is for SL1 connectivity (signal), blue for PWR connectivity (power) and grey for GND connections (ground). Figure adapted from [3].

2.2 Stackup

The structure has overall 11 cavities with planes, signal-layers and dielectrics. The planes are modeled as solid planes over the total size of the PCB. Inside the signal-layers the transmission lines are placed. If no transmission line is placed the space is filled with the same material as the dielectric. An overview of the stackup is shown in Tab. 3.

The connectivity of a layer is used to connect corresponding vias. Dielectric Material is not connected to any net. The Material definitions are shown in Tab. 4.

Table 3: Printed Circuit Board Stackup

Layer	**Type**	**Connectivity**	**Material**	**Thickness**
0	plane	GND	copper	1.0
1	dielectric	None	diel	6.0
2	plane	PWR	copper	1.0
3	dielectric	None	diel	4.0
4	plane	GND	copper	1.0
5	dielectric	None	diel	$TDIEL/2.0 - 0.5$
6	signal	SL1	copper	1.0
7	dielectric	None	diel	$TDIEL/2.0 - 0.5$
8	plane	GND	copper	1.0
9	dielectric	None	diel	$TDIEL/2.0 - 0.5$
10	signal	SL1	copper	1.0
11	dielectric	None	diel	$TDIEL/2.0 - 0.5$
12	plane	PWR	copper	1.0
13	dielectric	None	diel	$TDIEL/2.0 - 0.5$
14	signal	SL1	copper	1.0
15	dielectric	None	diel	$TDIEL/2.0 - 0.5$
16	plane	GND	copper	1.0
17	dielectric	None	diel	$TDIEL/2.0 - 0.5$
18	signal	SL1	copper	1.0
19	dielectric	None	diel	$TDIEL/2.0 - 0.5$
20	plane	GND	copper	1.0
21	dielectric	None	diel	$TDIEL/2.0 - 0.5$
22	signal	SL1	copper	1.0
23	dielectric	None	diel	$TDIEL/2.0 - 0.5$
24	plane	PWR	copper	1.0
25	dielectric	None	diel	$TDIEL/2.0 - 0.5$
26	signal	SL1	copper	1.0
27	dielectric	None	diel	$TDIEL/2.0 - 0.5$
28	plane	GND	copper	1.0
29	dielectric	None	diel	$TDIEL/2.0 - 0.5$
30	signal	SL1	copper	1.0
31	dielectric	None	diel	$TDIEL/2.0 - 0.5$
32	plane	GND	copper	1.0
33	dielectric	None	diel	4.0
34	plane	PWR	copper	1.0
35	dielectric	None	diel	6.0
36	plane	GND	copper	1.0

Table 4: Printed Circuit Board Material

Name	**Type**	**Conductivity** σ $\left(\frac{S}{m}\right)$	**Rel. Permittivity** ε_r	**Loss Tangent**	**Rel. Permeability** μ_r
diel	dielectric	Not Applicable	EPS	TAND	1.0
copper	conductor	58000000.0	Not Applicable	Not Applicable	1.0

2.3 Via

The vias have multiple dimensional aspects, an overview is given in Fig. 2. The dielectric material (Dielectric) is the material from the dielectric layer, see Tab. 3. Overall 3 different via models are being used, pwr_viamod, gnd_viamod and sig_viamod. Additional information of the parameters can be found in the CONMLS user manual CONMLS by TET).

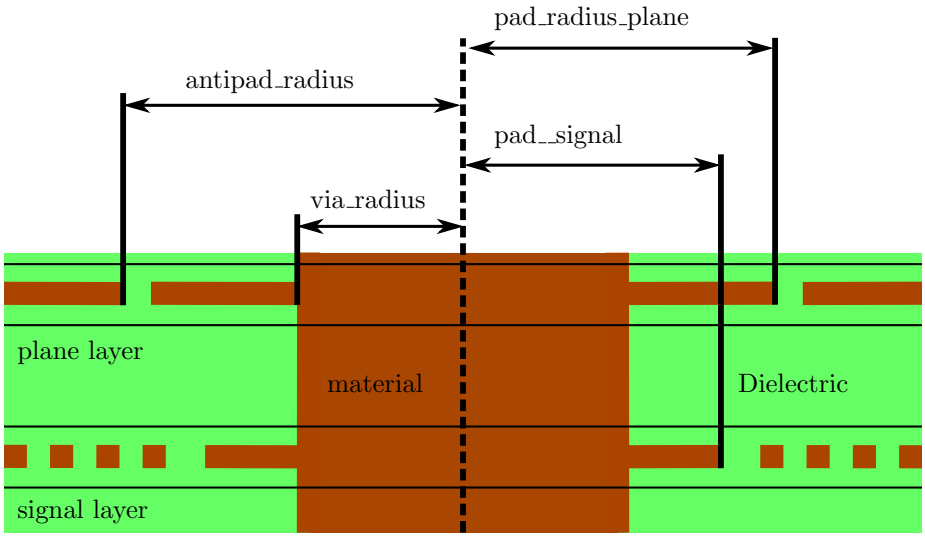

Figure 2: Overview of the via parameter e.g. via-radius. Pad radius signal and pad radius plane is relevant in the signal layer and plane layer respectively.

2.3.1 SIG Via: sig_viamod

The parameters of all sig vias are listed in Tab. 5. Signal vias without a connected transmission line are through vias from layer 0 to 36. Signal vias with a connected transmission line are blind vias from layer 0 to 6.

Table 5: Parameters Via Model: sig_viamod

Parameter	Value (mil)
name	sig_viamod
via_radius	VIAR
inner_radius	0.0
antipad_radius	ANTIPADR
pad_radius_plane	0.0
pad_radius_signal	0.0
cap_type	wg_junct
cap_fd	yes
cap_cfu	0.0
cap_cfl	0.0
material	copper

2.3.2 PWR Via: pwr_viamod

The parameters of all pwr vias are listed in Tab. 6. PWR vias are trough vias from layer 0 to 36 and are connected to all planes with PWR connectivity, see Tab. 3. The PWR vias are connected to the top and bottom most GND plane (layer 0 and layer 36) by a $5\,\Omega$ resistance.

Table 6: Parameters Via Model: pwr_viamod

Parameter	Value (mil)
name	pwr_viamod
via_radius	VIAR
inner_radius	0.0
antipad_radius	ANTIPADR
pad_radius_plane	0.0
pad_radius_signal	0.0
cap_type	wg_junct
cap_fd	yes
cap_cfu	0.0
cap_cfl	0.0
material	copper

2.3.3 GND Via: gnd_viamod

The parameters of all gnd vias are listed in Tab. 7. GND vias are trough vias from layer 0 to 36 and are connected to all planes with GND connectivity, see Tab. 3.

Table 7: Parameters Via Model: gnd_viamod

Parameter	Value (mil)
name	gnd_viamod
via_radius	VIAR
inner_radius	0.0
antipad_radius	ANTIPADR
pad_radius_plane	0.0
pad_radius_signal	0.0
cap_type	wg_junct
cap_fd	yes
cap_cfu	0.0
cap_cfl	0.0
material	copper

2.4 Via-Arrays

The via array is constructed by 3 different types of vias (GDN, PWR, signal), see Chap. 2.3. The vias are placed according to Fig. 1. Both via arrays are connected by 6 transmission lines, see Chap. 2.5.

2.5 Transmission Line

The transmission line is connecting two vias inside one signal layer. For the PCB all 6 transmission lines are inside the first signal layer (from top) layer 6, see Tab. 3. The thickness of the transmission lines is according to the stackup in table 3. The transmission line width is designed for a differential signaling. See Fig. 1 for the orientation of the transmission lines. Accordingly to the differential signaling the width of the transmission line is designed to result in a characteristic impedance of 100 Ω. The geometry of the tranmission line inside the via array is shown in Fig. 4. The parameters of the transmission line are listed in Tab. 8.

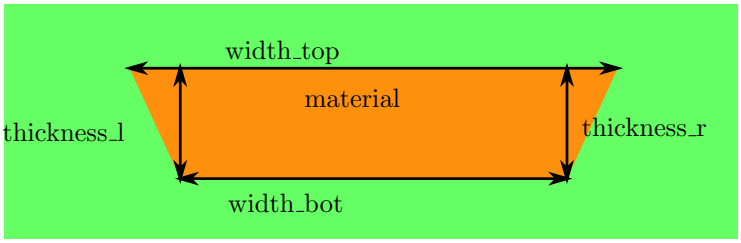

Figure 3: Cross Sections of the transmission line.

Table 8: Parameters Transmission Line Cross Section Geometry

Parameter	Value
width_top	TLWIDTH
width_bottom	TLWIDTH
thickness_r	1 mil
thickness_l	1 mil
material	copper

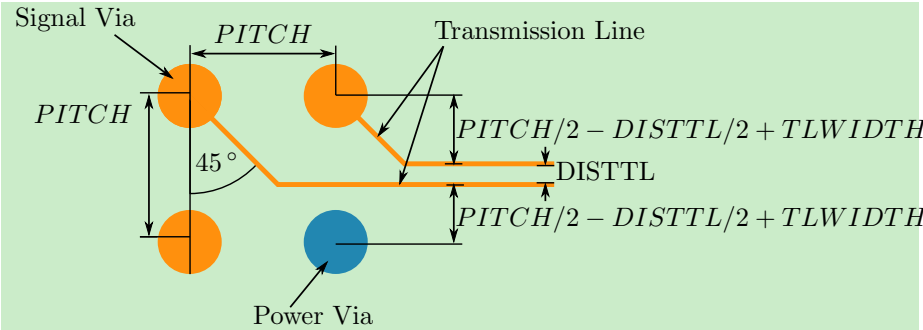

Figure 4: Top view of the geometry of the transmission lines inside the via array.

3 Parameter Variation

Some parameters of the PCB are varied throughout the EM simulations. Parameters are in general marked by capital letters. All parameter variations are stored in the file <parameter.csv>, see Chap. 3.1.

3.1 Parameter Storage File <parameter.csv>

The file <parameter.csv>is a tabular file with multiple columns (Delimeter = ',') and rows. The first row has all the parameter names as named in the tables and figures of this document. Each row is one EM simulation. By the column SIMU_INDEX the corresponding network parameters are found in the variation/ folder.

4 EM-Simulation

The EM simulations are carried out with an in house developed simulation tool. The tool is based on physics based via models [4–6]. In recent work of the institute many correlations with full-wave solver have been made with a high accuracy.

The simulations are performed with perfect matched layer (PML) boundary conditions. The frequency range is 5×10^8 Hz to 100×10^9 Hz with 200 linearly

separated frequency points.

5 Contact

You can find the contact information and the person in charge SI/PI-Database at TET): https://www.tet.tuhh.de/en/si-pi-database/

References

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