Link on 10 Cavity PCB with two 5x5 Via-Arrays

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I. Description

This link is placed on a printed circuit board (PCB) with two 5x5 via-arrays, as shown in Fig. 2. In the sixth cavity from top striplines are located which connect signal vias of both arrays, as shown in Fig. 2 (a). The connectivity of GND and signal vias is shown in Fig 2 (b), with a via ratio of 2 : 1 for signal and GND, respectively. At each via two ports are placed one at the top (odd numbers) of the PCB and one at the bottom (even numbers) . A more thoroughly description is given in [1].

All planes of the stackup are connected by GND vias. The radius of the via barrel is smaller than the radius of the via pads on top and bottom of the stackup, as shown in Fig. 2 (a). All pad of the signal vias are exactly as the via radius (via_radius). All plane pad radius are exactly the via radius except for the top most and bottom most planes. An additional parameter is the array distance, which represents the distance between the two via-arrays.

II. Modeling Tool

All simulations have been carried out with a physics-based (PB) approach [2]–[4]. ~~A demo version of the tool can be accessed at ***www.tet.tuhh.de***.~~ All information regarding the setup are described in the following.

III. Parameter

If a value is given in the tables the parameter is not altered during the simulations. On the other hand if the value is varied the according entry of the $< parameter.csv >$ file is given.

A. Via Model

The dimensions of the vias used in the structure shown in Fig. 2 are given in Fig. 1. All vias are based on this model. For the dielectric material (Dielectric) the rel. permittivity (ε_r) and the loss tangent ($\tan\delta$) are given. For the conductive material (Metal) the conductivity (σ) is given. An overview is given in Tab. I.

Table I: Overview of the parameters used in the via model, as shown in Fig. 1

Parameter	Value
via radius	via_radius
antipad radius	antipad_radius
pad radius plane	pad_radius
pad radius signal	via_radius

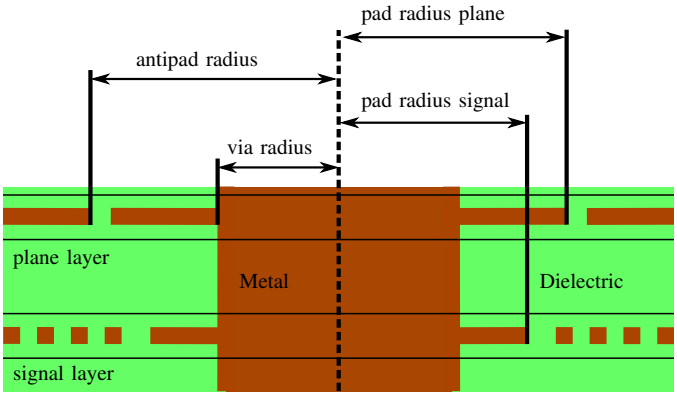
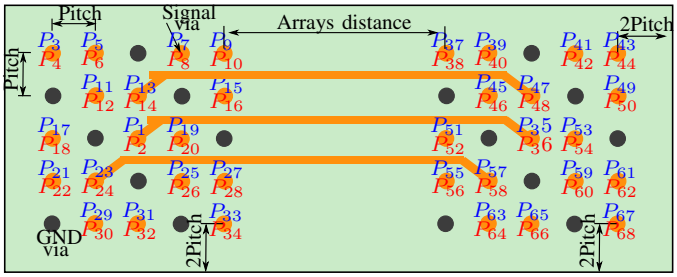
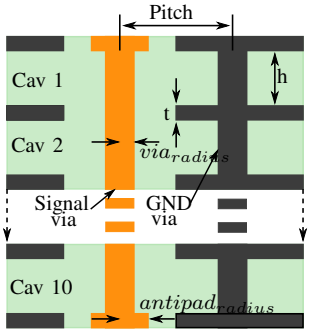


Fig. 1: Via model used for all vias of the structure. If the radius values are not given the via_radius is used for pad_radius_plane, and pad_radius_signal.



(a)



(b)

Fig. 2: (a) is the top view in the 5x5 via-array, (b) is the stackup. GND vias are connected to all ground planes. The ports are placed on top and bottom of the PCB. Top ports are blue (odd numbers), bottom ports are red (even numbers).

B. Materials

Two different materials were used, the material for the metal e.g. planes, striplines, vias, pads, and the material for the

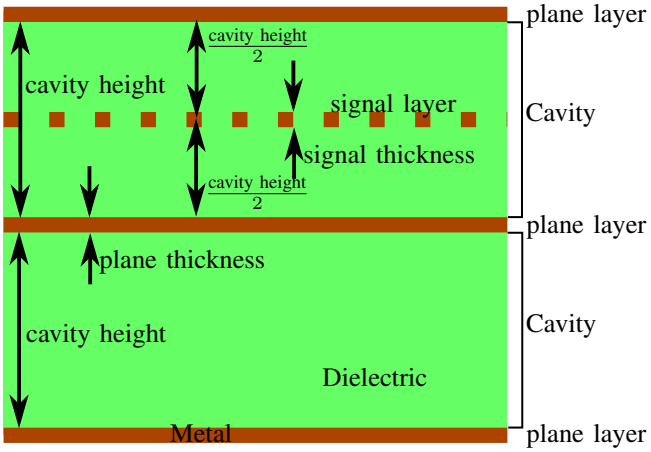


Fig. 3: Stackup nomenclature for the problem. The naming refers to all cavities unless stated differently in the description.

dielectric e.g. cavity filling, antipad. The metal requires two parameter conductivity (σ) and rel. permeability (μ_r). The dielectric has the rel. permittivity (ε_r) and the loss tangent ($\tan\delta$). An overview is given in Tab. II.

Table II: Overview of the material parameters used in the structure.

Parameter	Value
σ	1×10^{30} S/m
μ_r	1
ε_r	epsilon_r
$\tan\delta$	loss_tangent

C. Stackup

For the stackup general parameters are introduced. If not stated differently in the description the naming refers to all cavities of the stackup. One cavity is defined by the enclosed dielectric material by two planes, as shown in Fig. 3. Signal layers are defined in the middle of the cavity. The cavity height is the distance between two plane layers (here cavity_height).

Table III: Overview of the parameters related to the stackup used in the PCB.

Parameter	Value
cavity height	cavity_height
plane thickness	plane_thickness
signal thickness	plane_thickness

D. Via Model

All striplines are in the center of a cavity. and are defined by the width and the thickness, as shown in Fig. 4. All striplines are based on this model. For the dielectric material (Dielectric) the rel. permittivity (ε_r) and the loss tangent ($\tan\delta$) are given. For the conductive material (Metal) the conductivity (σ) is given. An overview is given in Tab. IV.

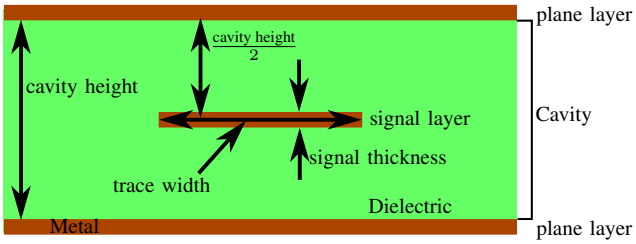


Fig. 4: Stripline model for all striplines used in the PCB.

Table IV: Overview of the parameters used in the via model, as shown in Fig. 4

Parameter	Value
signal thickness	plane_thickness
trace width	trace_width

E. File <parameter.csv>

The file $< parameter.csv >$ has all necessary information for the setup of the geometry and parameter variations. The columns are:

- index
- simuIndex
- antipad_radius
- via_radius
- via_pitch
- cavity_height
- epsilon_r
- loss_tangent
- trace_width
- array_distance
- pad_radius
- plane_thickness

Index is the row in the $< parameter.csv >$, cavity_height is the distance between the two metal planes, epsilon_r is the relative permittivity (ε_r) of the dielectric between the power and ground planes, loss_tangent is $\tan(\delta)$ of the dielectric, via_pitch is the distance between vias in the array, pad_radius is the radius of the via pad on top and bottom of the PCB, antipad_radius is the radius of the cutout (via hole) around a via, trace_width is the width of each trace connecting the arrays, array_distance is the distance between the arrays, simuIndex is the simulation index (<index>) to find the simulation results, via_radius is the radius of the via barrel, plane_thickness is the thickness of the GND plane layers.

IV. Publications

This structure was used in [1].

References

[1] A. S. Masís, A. Carmona-Cruz, M. Schierholz, X. Duan, K. Roys, C. Yang, R. Rimolo-Donadio, and C. Schuster, "Generation of Via Interconnect Classification Models with Feed-Forward Neural Networks assisted by Genetic Algorithms," *to be submitted to 2021 IEEE 25th Workshop on Signal and Power Integrity (SPI)*, Jul. 2021.

[2] R. Rimolo-Donadio, X. Gu, Y. Kwark, M. Ritter, B. Archambeault, F. de Paulis, Y. Zhang, J. Fan, H.-D. Brüns, and C. Schuster, "Physics-Based Via and Trace Models for Efficient Link Simulation on Multilayer Structures Up to 40 GHz," *IEEE Transactions Microwave Theory and Techniques*, vol. 57, no. 8, pp. 2072–2083, Aug. 2009.

[3] S. Müller, X. Duan, M. Kotzev, Y.-J. Zhang, J. Fan, X. Gu, Y. H. Kwark, R. Rimolo-Donadio, H.-D. Brüns, and C. Schuster, "Accuracy of Physics-Based Via Models for Simulation of Dense Via Arrays," *IEEE Transactions on Electromagnetic Compatibility*, vol. 54, no. 5, pp. 1125–1136, Oct. 2012. [Online]. Available: https://doi.org/10.1109/temc.2012.2192123

[4] S. Müller, F. Happ, X. Duan, R. Rimolo-Donadio, H.-D. Bruns, and C. Schuster, "Complete Modeling of Large Via Constellations in Multilayer Printed Circuit Boards," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 3, no. 3, pp. 489–499, Mar. 2013. [Online]. Available: https://doi.org/10.1109/tcpmt.2012.2234211