PWR/GND Plane PCB with 11x11 Via-Array

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I. Description

This structure consists of a power delivery network (PDN) on a PCB with one cavity, a power plane on the bottom and a ground plane on top, as shown in Fig. 1 (b). A more detailed description is given in [11], [12]. Port 1 is in the center of a via-array and is the port that is decoupled by placing decoupling capacitors (decaps) on the surrounding via array. The distance of vias inside the via array ($via-pitch$) is 40 mil. At the center of the array (Port 1) the impedance of the PDN is observed. With this configuration the impact of decaps on the PDN impedance was investigated. The variations for this structure include changing the distance of the planes, the material properties and the decaps. For the decaps the location, capacitance and number was varied. The capacitors were chosen from a library containing overall 15 values including equivalent series resistance and equivalent series inductance.

II. Modeling Tool

All simulations have been carried out with a physics-based (PB) approach [1]–[3]. A demo version of the tool can be accessed over ***www.tet.tuhh.de***. All information regarding the setup are described in the following.

III. Parameter

If a value is given in the tables the parameter is not altered during the simulations. On the other hand if the value is varied the according entry of the $< parameter.csv >$ file is given.

A. Via Model

The dimensions of the vias used in the structure shown in Fig. 1 are given in Fig. 2. All vias are based on this model. For the dielectric material (Dielectric) the rel. permittivity (ε_r) and the loss tangent ($\tan\delta$) are given. For the conductive material (Metal) the conductivity (σ) is given. An overview is given in Tab. I.

Table I: Overview of the parameters used in the via model, as shown in Fig. 2

Parameter	Value
via radius	5 mil
antipad radius	18 mil
pad radius plane	5 mil
pad radius signal	5 mil

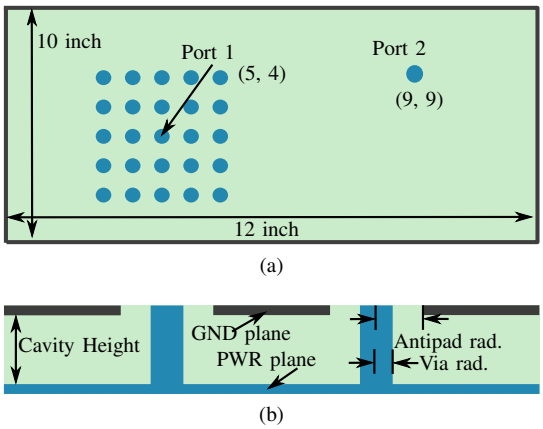

Fig. 1: For clarity the size of the via array is increased and the number of vias is reduced. The center of the via array is the port under investigation. All dimensions are in inch. (a) top view, (b) cross view. Figures adapted from [4].

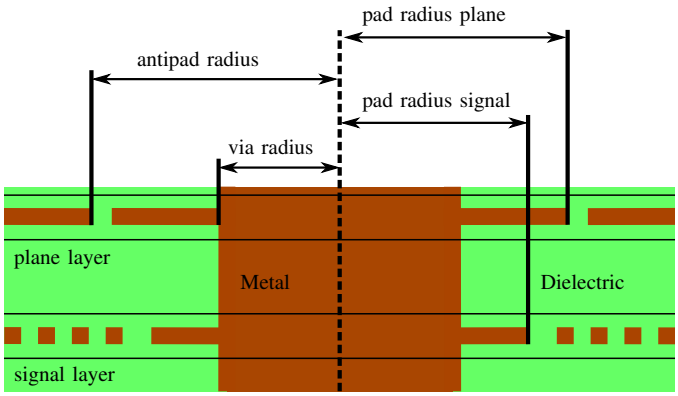

Fig. 2: Via model used for all vias of the structure. If the radius values are not given the via_radius is used for pad_radius_plane, and pad_radius_sgnal.

B. Materials

Two different materials were used, the material for the metal e.g. planes, striplines, vias, pads, and the material for the dielectric e.g. cavity filling, antipad. The metal requires two parameter conductivity (σ) and rel. permeability (μ_r). The dielectric has the rel. permittivity (ε_r) and the loss tangent ($\tan\delta$). An overview is given in Tab. II.

C. Stackup

For the stackup general parameters are introduced. If not stated differently in the description the naming refers to all

Table II: Overview of the material parameters used in the structure.

Parameter	Value
σ	conductivity
μ_r	1
ε_r	epsilon_r
$\tan\delta$	loss_tangent

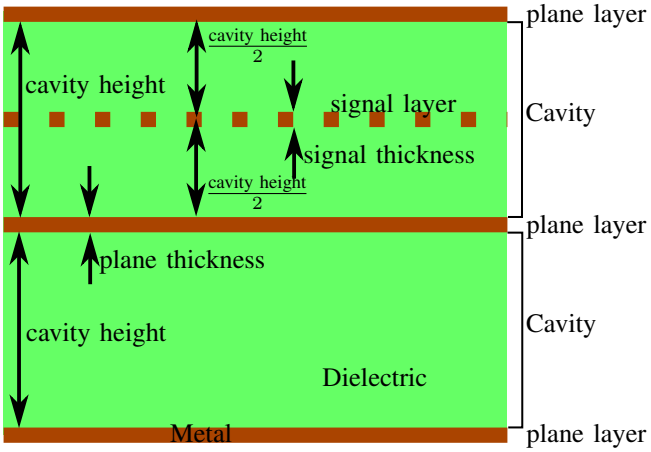

Fig. 3: Stackup nomenclature for the problem. The naming refers to all cavities unless stated differently in the description.

cavities of the stackup. One cavity is defined by the enclosed dielectric material by two planes, as shown in Fig. 3. Signal layers are defined in the middle of the cavity. The cavity height is the distance between two plane layers (here diel_height).

Table III: Overview of the parameters related to the stackup used in the printed circuit board (PCB).

Parameter	Value
cavity height	diel_height
plane thickness	1 mil
signal thickness	1 mil

D. File <*parameter.csv*>

The file <*parameter.csv*> contains all necessary information for the setup of the geometry and parameter variations. The columns are:

- index
- diel_height (Cavity Height)
- epsilon_r
- loss_tangent
- conductivity
- ic_x (of Port 1)
- ic_y (of Port 1)
- simuIndex
- {ESR/ESL/C/xPos/yPos}

Index is the row in the <*parameter.csv*>, diel_height is the distance between the two metal planes, epsilon_r is the relative permittivity (ε_r) of the dielectric between the power and ground planes, loss_tangent is $\tan(\delta)$ of the dielectric, conductivity is the conductivity of the planes and the via material, [ic_x and ic_y] is the center of the via-array, simuIndex is the simulation index (<simuIndex>) to find the simulation results in the variation folder. The last column ({ESR/ESL/C/xPos/yPos}) is a list of the placed capacitors. For each capacitor the equivalent series resistance (ESR), equivalent series inductance (ESL), capacitance (C), absolute x position on the PCB and absolute y position on the PCB is given. As delimiter "/" (slash) is chosen.

E. File <*preproc_parameter.csv*>

The file <*preproc_parameter.csv*> contains all necessary information for the setup of the geometry and parameter variations. This file can be used directly for a machine learning application The columns are:

- diel_height (Cavity Height)
- epsilon_r
- loss_tangent
- conductivity
- ic_x (of Port 1)
- ic_y (of Port 1)
- sector values
- targetMet

Index is the row in the <*preproc_parameter.csv*>, diel_height is the distance between the two metal planes, epsilon_r is the relative permittivity (ε_r) of the dielectric between the power and ground planes, loss_tangent is $\tan(\delta)$ of the dielectric, conductivity is the conductivity of the planes and the via material, [ic_x and ic_y] is the center of the via-array. The columns sector values contain the preprocessed decap positions according to [4] with a ring-sector-method with linear spacing. Except for the last column targetMet all columns are input features. targetMet is an expectation value. If the target impedance (TI) is violated the value is 0, 1 otherwise.

IV. Publications

This structure was used in [4], [5]. In both publications investigations with respect to machine learning (ML) techniques were made.

References

[1] R. Rimolo-Donadio, X. Gu, Y. Kwark, M. Ritter, B. Archambeault, F. de Paulis, Y. Zhang, J. Fan, H.-D. Brüns, and C. Schuster, "Physics-Based Via and Trace Models for Efficient Link Simulation on Multilayer Structures Up to 40 GHz," *IEEE Transactions Microwave Theory and Techniques*, vol. 57, no. 8, pp. 2072–2083, Aug. 2009.

[2] S. Müller, X. Duan, M. Kotzev, Y.-J. Zhang, J. Fan, X. Gu, Y. H. Kwark, R. Rimolo-Donadio, H.-D. Brüns, and C. Schuster, "Accuracy of Physics-Based Via Models for Simulation of Dense Via Arrays," *IEEE Transactions on Electromagnetic Compatibility*, vol. 54, no. 5, pp. 1125–1136, Oct. 2012. [Online]. Available: https://doi.org/10.1109/temc.2012.2192123

[3] S. Müller, F. Happ, X. Duan, R. Rimolo-Donadio, H.-D. Bruns, and C. Schuster, "Complete Modeling of Large Via Constellations in Multilayer Printed Circuit Boards," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 3, no. 3, pp. 489–499, Mar. 2013. [Online]. Available: https://doi.org/10.1109/tcpmt.2012.2234211

[4] C. M. Schierholz, K. Scharff, and C. Schuster, “Evaluation of Neural Networks to Predict Target Impedance Violations of Power Delivery Networks,” in *Proceedings IEEE 28th Conf. Electrical Performance Electronic Packaging and Systems EPEPS*, Montreal, CA, Oct. 2019.

[5] M. Schierholz, C. Yang, K. Roy, M. Swaminathan, and C. Schuster, “Comparison of Collaborative versus Extended Artificial Neural Networksfor PDN Design,” in *Proceedings 2020 IEEE 24th Workshop on Signal and Power Integrity (SPI)*, May 2020. [Online]. Available: https://doi.org/10.1109/spi48784.2020.9218157