6-Layer PCB based PDN with Two Via Arrays - Latin Hypercube Sampling

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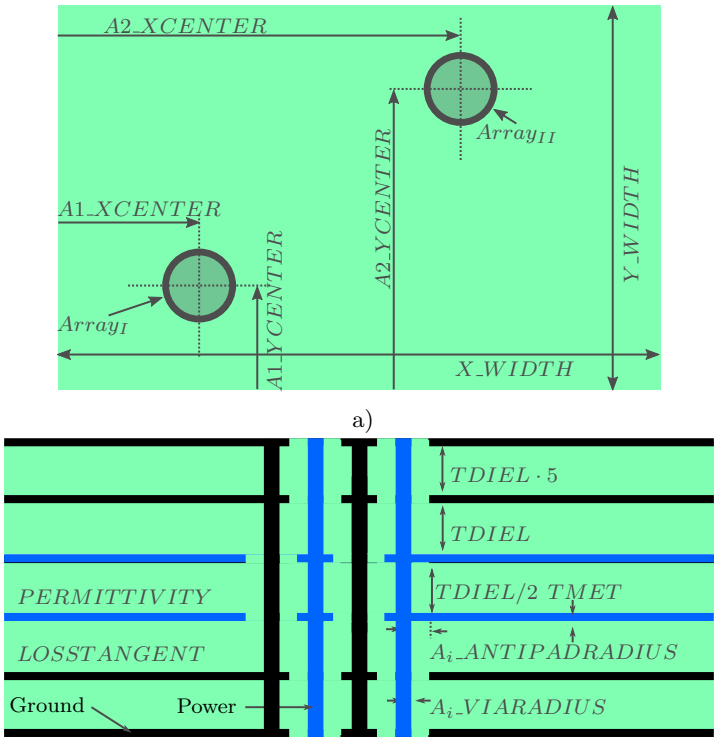

Figure 1: a) Top view of the printed circuit board (PCB), b) side view of the printed circuit board (PCB). The parameters are named as found in the data files. The array are numbered $A1$, $A2$, and additional a voltage regulator module array is present on the board. The board number $A1$ or VRM is used as prefix for the array dependent parameter, e.g. via radius.

1 Introduction

You can find all information regarding the printed circuit board (PCB) structure and setup in the following chapters. The PCB is described by the stackup, (order, type, material, thickness of layers) the board geometry (height, width), the via geometry (via radius, via antipad, etc.), the transmission lines (width, thickness, material) only if applicable and connectivity of vias, planes and [transmissions lines].

Each of the previously mentioned aspects has an individual chapter. If instead of an numerical value a variable (capital letters) is given this parameter is varied during the electromagnetic (EM) simulations. Further information are found in Chap. 3.

1.1 How to Cite?

If you use the provided data you have to reference by using at least the following Open Access paper [1]:

> M. Schierholz et al., "SI/PI-Database of PCB-Based Interconnects for Machine Learning Applications," in IEEE Access, vol. 9, pp. 34423-34432, 2021, doi: 10.1109/ACCESS.2021.3061788.

1.2 Data Structure

Included in the download are multiple files and folders, See Tab. 1. See Fig. 1 for the parameter definitions.

Table 1: Data Directory

Name	**Type**	**Description**
ReadMe.pdf	PDF-Document	This Description
parameter.csv	CSV Document (Delimeter = ',')	Parameter file with all parameter variations, see Chap. 3.
variation/	Directory	Directory having all EM simulation results (S-Parameter), see Chap 4

Table 2: Printed Circuit Board Shape

Height (mil)	**Width (mil)**
[YWIDTH]	[XWIDTH]

Table 3: Printed Circuit Board Stackup

Layer	**Type**	**Connectivity**	**Material**	**Thickness**
0	plane	GND	copper	[TMET]
1	dielectric	None	dielmoat	$[TDIEL] \cdot 5.0$
2	plane	GND	copper	[TMET]
3	dielectric	None	dielmoat	[TDIEL]
4	plane	PWR	copper	[TMET]
5	dielectric	None	dielmoat	[TDIEL]/2.0
6	plane	PWR	copper	[TMET]
7	dielectric	None	dielmoat	[TDIEL]
8	plane	GND	copper	[TMET]
9	dielectric	None	dielmoat	$[TDIEL] \cdot 5.0$
10	plane	GND	copper	[TMET]

2 PCB Structure

The structure is a PCB with multiple planes, vias and materials. The vias and the stackup is explained in the following sections. If a parameter (italic font) instead of a numerical value is given this parameter was changed during the EM simulation. Further information of the parameters are found in Chap. 3.

2.1 Board Size

The height and width of the PCB is listed in Tab. 2.

2.2 Stackup

The structure has overall 5 cavities with planes, and dielectrics. The planes are modeled as solid planes over the total size of the PCB. An overview of the stackup is shown in Tab. 3.

The connectivity of a layer is used to connect corresponding vias. Dielectric Material is not connected to any net. The Material definitions are shown in Tab. 4.

2.3 Via

The vias have multiple dimensional aspects, an overview is given in Fig. 2. The dielectric material (Dielectric) is the material from the dielectric layer, see Tab. 3. For each via array different via parameters are possible e.g. via radius.

Table 4: Printed Circuit Board Material

Name	**Type**	**Conductivity** σ $\left(\frac{S}{m}\right)$	**Rel. Permittivity** ε_r	**Loss Tangent**	**Rel. Permeability** μ_r
copper	conductor	[CONDUCTIVITY]	not applicable	not applicable	1.0

Additional information of the parameters can be found in the CONMLS user manual CONMLS by TET).

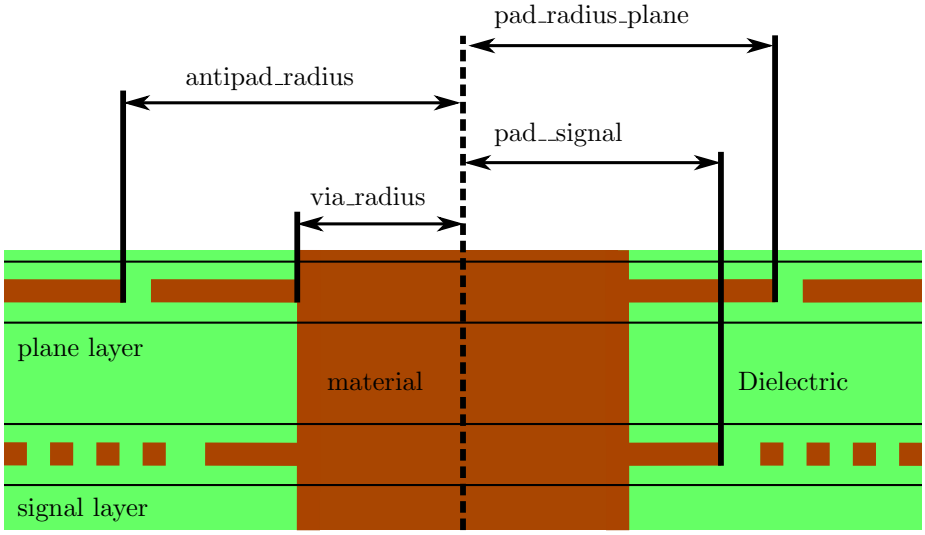

Figure 2: Overview of the via parameter e.g. via-radius. Pad radius signal and pad radius plane is relevant in the signal layer and plane layer respectively.

2.3.1 A1: Via Model and Array

The vias of array $A1$ are organized in an interstitial pattern with $3x3$ power vias and $4x4$ ground vias, see Fig. 3 a) and b). All ground vias are connected to all ground planes. All power vias are connected to all power planes. The pitch is defined according to Fig. 3 a) and b), top, and bottom view, respectively.

2.3.2 A2: Via Model and Array

The vias of array $A2$ are organized in an interstitial pattern with $3x3$ power vias and $4x4$ ground vias, see Fig. 3 c) and d). All ground vias are connected to all

Table 5: Parameters Via Model: a2_via_model

Parameter	**Value (mil)**
name	a2viamodel
via_radius	[A2_VIARADIUS]
inner_radius	0.0
pad_radius_signal	0.0
antipad_radius	[A2_ANTIPADRADIUS]
pad_radius_plane	0.0
material	copper
cap_type	auto
cap_fd	no
cap_cfu	0.0
cap_cfl	0.0

ground planes. All power vias are connected to all power planes. The pitch is defined according to Fig. 3 c) and d), top, and bottom view, respectively.

Table 6: Parameters Via Model: a2_via_model

Parameter	**Value (mil)**
name	a2viamodel
via_radius	[A2_VIARADIUS]
inner_radius	0.0
pad_radius_signal	0.0
antipad_radius	[A2_ANTIPADRADIUS]
pad_radius_plane	0.0
material	copper
cap_type	auto
cap_fd	no
cap_cfu	0.0
cap_cfl	0.0

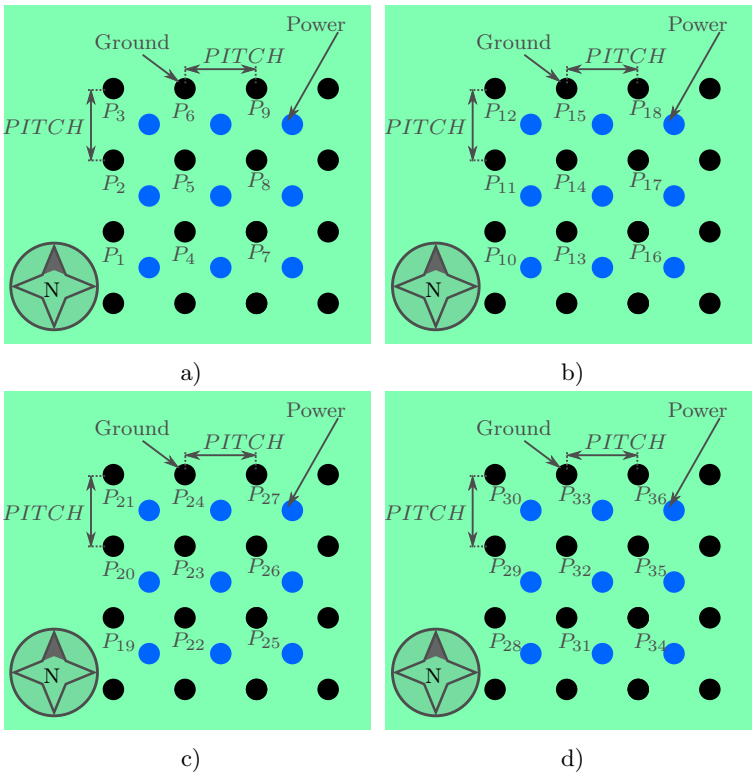

Figure 3: a) top view of $A1$ with interstitial pattern and port numbering. b) bottom view of $A1$ with interstitial pattern and port numbering. c) top view of $A2$ with interstitial pattern and port numbering. d) bottom view of $A2$ with interstitial pattern and port numbering.

3 Parameter Variation

Some parameters of the PCB are varied throughout the EM simulations. Parameters are in general marked by capital letters. All parameter variations are stored in the file <parameter.csv>, see Chap. 3.1.

3.1 Parameter Storage File <parameter.csv>

The file <parameter.csv>is a tabular file with multiple columns (Delimeter = ',') and rows. The first row has all the parameter names as named in the tables and figures of this document. Each row is one EM simulation. By the column SIMU_INDEX the corresponding network parameters are found in the variation/ folder.

4 EM-Simulation

The EM simulations are carried out with an in house developed simulation tool. The tool is based on physics based via models [2–4]. In recent work of the institute many correlations with full-wave solver have been made with a high accuracy.

The simulations are performed with perfect magnetic conducting (PMC) boundary conditions. The frequency spectrum is 1×10^6 Hz to 1×10^9 Hz with 334 linearly spaced frequency points.

5 Contact

You can find the contact information and the person in charge SI/PI-Database at TET): https://www.tet.tuhh.de/en/si-pi-database/

References

[1] M. Schierholz, A. Sanchez-Masis, A. Carmona-Cruz, X. Duan, K. Roy, C. Yang, R. Rimolo-Donadio, and C. Schuster, "SI/PI-database of PCB-based interconnects for machine learning applications," *IEEE Access*, vol. 9, pp. 34 423–34 432, Feb. 2021.

[2] R. Rimolo-Donadio, X. Gu, Y. Kwark, M. Ritter, B. Archambeault, F. de Paulis, Y. Zhang, J. Fan, H.-D. Brüns, and C. Schuster, "Physics-Based Via and Trace Models for Efficient Link Simulation on Multilayer Structures Up to 40 GHz," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 8, pp. 2072–2083, Aug. 2009.

[3] X. Duan, R. Rimolo-Donadio, H.-D. Brüns, and C. Schuster, "A Combined Method for Fast Analysis of Signal Propagation, Ground Noise, and Radiated Emission of Multilayer Printed Circuit Boards," *IEEE Transactions on Electromagnetic Compatibility*, vol. 52, no. 2, pp. 487–495, May 2010. [Online]. Available: https://doi.org/10.1109/temc.2010.2041238

[4] S. Müller, F. Happ, X. Duan, R. Rimolo-Donadio, H.-D. Bruns, and C. Schuster, "Complete Modeling of Large Via Constellations in Multilayer Printed Circuit Boards," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 3, no. 3, pp. 489–499, Mar. 2013. [Online]. Available: https://doi.org/10.1109/tcpmt.2012.2234211