Fast Simulations of Nonlinearly Loaded Large-Scale Systems via Reduced Order Models

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Work Report

Ph.D. Research Activity

by

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Outline

1. Project Description

The following project aims to contribute two fields of applications

- Model Order Reduction (compression of large-scale mixed linear/nonlinear dynamical systems)
- Numerical simulation of electrically large electromagnetic structures terminated on NL loads

The main question that this research activity wants to answer is

can we apply a model-order-reduction technique to reduce the simulation costs given by the interaction of a large size dynamical system with nonlinear terminations, by reducing the number of variables at play during a time-domain simulation?

State-of-the-art

Since the 1970s, when the starting point was a single wire antenna loaded with a diode [1], the simulation of electrical/electromagnetic structures with nonlinear terminations is major topic of interest in the academia. Since the first case of study, the applications complexity has grown during the years. Examples are active antennas [2], grid amplifiers [3], amplifier with shielding structures [4], on-chip interconnects with NL terminations [5], multistage amplifiers [6], and PCB decoupling problems. Recently, the interest in energy selective meta-surfaces provides a new challenge in the field of circuit-simulations, ranging from meta-surface absorbers [7], [8], energy selective shielding [9], to nonlinear impedance surfaces [10].
The general trend over the years shows dynamical systems of increasing size, massively loaded with NL components.
The simulation approaches for such structures can be generally classified into two classes

1. full time domain solvers; Examples are the time-domain finite-element method [11], the FIT [9], or the transmission line modelling [11];
2. hybrid techniques based on nonlinear equations related to the time-domain (or proper circuit solvers), to deal with the NL components, combined with a full-wave or a frequency-domain based solver for the passive structure; these approaches include the combination of Method of Moments (MoM) and time-matching [1], Volterra series analysis [12] and harmonic balance [13].

This project belongs to the second class. The main goal is to apply Model Order Reduction (MOR) techniques to fast simulation of a large-scale mixed linear/nonlinear dynamical system.
MOR is a well-developed cross-application discipline, which led over the years to the development of several algorithms that, given a large-scale system produces a more compact model by preserving accuracy and other features of interest (stability, passivity, etc.)
Nowadays, the most relevant algorithm for the approximation of a linear system starting from a set of frequency responses is the Vector Fitting (VF) algorithm [14]. VF is well established both in academic and industrial communities due its main features: with this approach the extraction of a rational approximation of a multiport system in a passive state-space macromodel, that can be synthesized into an equivalent netlist suitable for any circuit solver [15], is a straightforward task. A modified version of the VF able to deal with large-scale structures was proposed in [16], with a remarkable speed-up of the entire

procedure. Nevertheless, standard approaches to deal with the macromodel passivity [15], [17], [18] reveal to be inefficient for such type of applications.

For the application of a MOR approach to the NL part of the dynamical system several approaches are currently available in the literature [19]. Among the others, proper orthogonal decomposition (POD) [15], [20] appears to be the most reliable for the approximation of a strongly nonlinear circuit. Nevertheless, its main drawbacks are related to the complexity of the resulting ROM and to the necessity of the computation of a nonlinear function, and its Jacobian, in a transient simulation. Other approaches are based on the acquisition of a set of selected spatial points of the nonlinear functions to be approximated, reducing the main cost associated to the evaluation of the Jacobian. Within this class, we mention the Empirical Interpolation Method (EIM) [21] and its variant, the discrete EIM (DEIM) [22]. Both these strategies present promising results but, up to present, they have been specifically focused on systems obtained from the discretization of nonlinear partial differential equations (PDEs). This last aspect limits the range of applications required in our context.

A recent paper [23] presents an algorithm based on POD, with the support of an interpolatory component, for the simulation of the nonlinear transmission lines. The authors claim that the interpolatory-POD (IPOD) could be applied irrespectively to the topology of the circuit or the type of nonlinear components. Nevertheless, to the best of our knowledge, the application of a robust and reliable MOR technique to a large-scale nonlinear problem is still an open topic.

2. Tasks and Milestones

The aim of this project is improving the state-of-the-art in numerical simulation of large electrical/electromagnetic structures massively loaded with NL components/terminations. Examples are meta-surfaces for nonlinear shielding, or power delivery networks in Printed Circuit Boards (PCBs). The interplay between distributed (electrically large) nature and presence of NL terminations make the numerical simulation problem (to be cast in time-domain) extremely challenging. Our main effort is dedicated to address two major limitations of state-of-the-art mixed circuit/field simulation methods, with specific reference to approaches based on model-order-reduction (macromodeling):

- Improve and streamline generation of compact, passive and reliable macromodels for large-scale components, with hundreds of ports, obtained from tabular frequency responses
- Systematic extraction and inclusion of reduced-order models also for the nonlinear terminations in a dedicated simulation environment, when the number of NL loads becomes very large.

The tasks of the project and the corresponding milestones are summarized as follows:

1. Enhancement and testing of a fully reliable workflow for the extraction of stable, passive and sparse reduced-order models of electrically large linear structures, using a standard low-performance hardware (laptop), ensuring good scalability with the size of the problem at hand;
    - Rational approximation algorithms (e.g. VF) are currently the state-of-the-art with strong limitations for large-size cases, but the recent contributions (and the ongoing research) of POLITO group in the passivity check/enforcement

field provided, by the time the scholarship started, a significant improvement in this area, strongly attenuating the current main limitation associated to the model passivity property;
    - TUHH provided benchmarks and different applications to be used for the validation of the current research; a proper set of test-cases (with a significant and various number of frequency responses) is fundamental to stress the algorithm under development by POLITO and for the certification of the following items;

2. Assessment of the robustness of the simulation engine based on the Waveform-Relaxation (WR) scheme, created by TUHH, on other type of benchmarks with respect to the meta-surfaces used for the tool development; indeed, we believe that its extension and usage to other applications could open future research directions, allowing us to verify the outcomes of point 3 below, and eventually build a completely novel simulation environment;

3. The investigation of a novel approach for the realization of a reduced order model of the large-scale NL terminations, which are usually interconnected to the linear part of the system with a specific (and replicated) pattern, to be embedded in a standard circuit simulation; this item requires
    a. a stable (and passive) model realization based on a compression technique, that takes advantage of the spatial correlation between loads to obtain a projection onto a lower-dimensional subspace. Examples are as DEIM [22] or even much simpler (but effective) approaches, like an iterative polynomial approximation, or the well-established POD (in its more advanced format in [23]).
    b. a model synthesis in a standard form or an ad hoc simulation framework able to deal with the ROM model of the nonlinear part, such as a modified version of the WR tool developed by TUHH;
    c. a sufficient number of benchmarks to be used for the validation and a comparison campaign of different methodologies regarding the above points; indeed, this provides a milestone to be used for future research efforts in the field;

3. Investigation and Achievements

Here follows a summary of the investigation carried out during my stay at TUHH, including failures and achievements. Indeed, a dedicated section addresses each of the three tasks described above, documenting results and providing examples.

Task 1

During my time at TUHH, a reliable workflow has been verified to generate accurate, stable, and passive models of electrically large structures, scaling with the size of the problem at hand.

In particular, the effectiveness of the proposed modeling approach has been tested on meta-surfaces with many interconnections, building accurate models of systems with 9, 25, 100, 225, 400 and 1024 ports, as well as transmission lines up to 400 ports.

Figure 1 shows the accuracy of a passive model with 1024 ports build following the proposed macromodeling procedure, fully documented in [24].

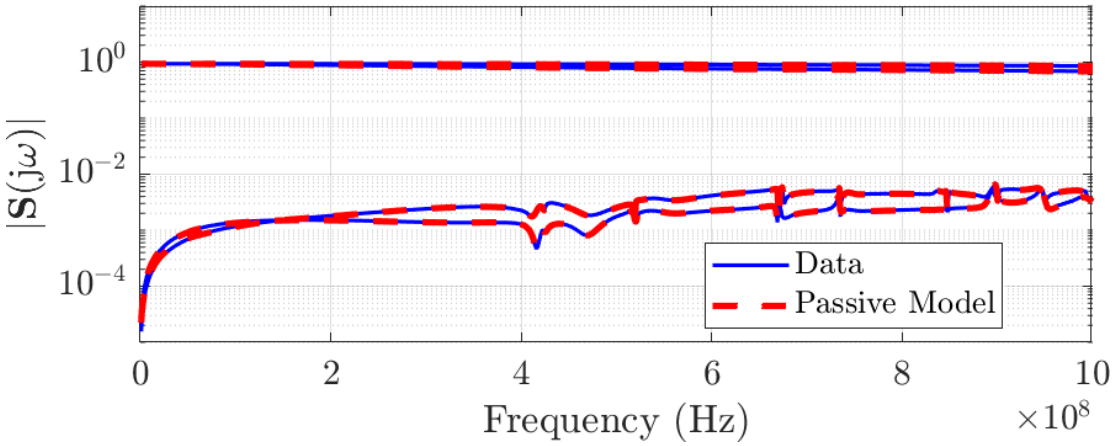


Figure 1. Modelling a 1024-port shielding enclosure: passive macromodel accuracy on selected responses.

To obtain this result, the original MoM data provided by TUHH have been regularized and extrapolated up to DC following the procedure preliminary documented in [25] (and finalized in [24]), a VF model has been build following [16], and finally a passive result has been obtained using the proposed passivity enforcement (PE) scheme based on an adaptive sampling procedure [26]. The maximum singular values of the model responses $\sigma_{max}\{\mathrm{H}(j\omega)\}$ before and after are reported in Figure 2.

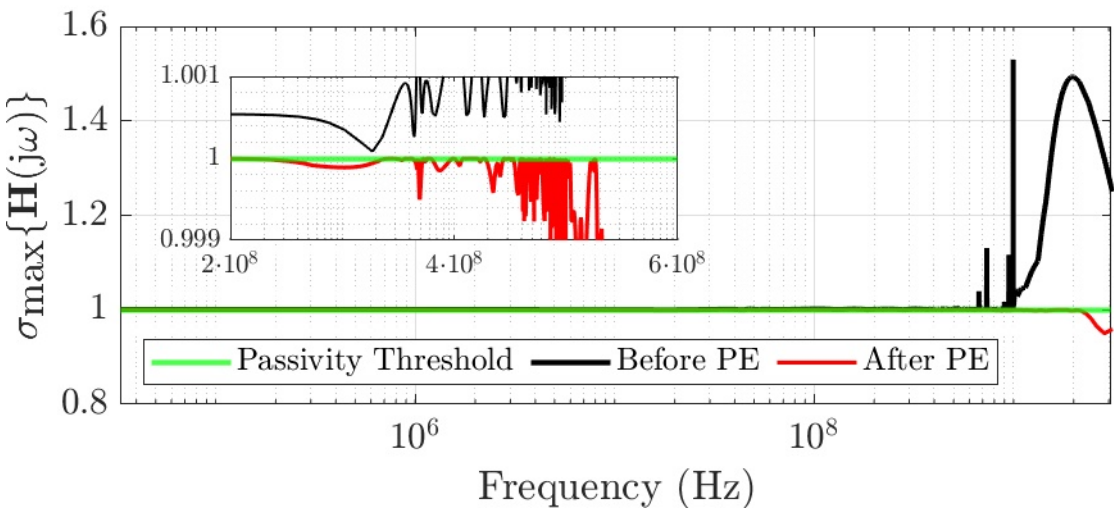


Figure 2. Passivity of a 1024-port model before and after the proposed Passivity Enforcement (PE) scheme.

We recall that in order to be passive (i.e. numerically stable during transient circuit simulations) the condition $\sigma_{max}\{\mathrm{H}(j\omega)\} < 1$ must hold $\forall\omega \in [0, \infty)$.

To obtain the result documented above, the proposed procedure required ≈ 119 seconds for the model generation (including data compression) and ≈ 44.3 hours for the passivity enforcement. Please notice that obtaining a model with the presented complexity (1024

ports and 71 poles, for an overall number of 72704 states) with a standard tool (e.g. [27]) is practically unfeasible without decreasing the number of poles (i.e. the number of model decision variables) and reducing the overall accuracy requirements.

Figure 3 summarizes the same results for a 400-port box. A passive model with 79 poles (31600 states) has been obtained after a total of ≈ 4.3 hours, considering all procedure steps (data compression, model fitting and passivity enforcement).

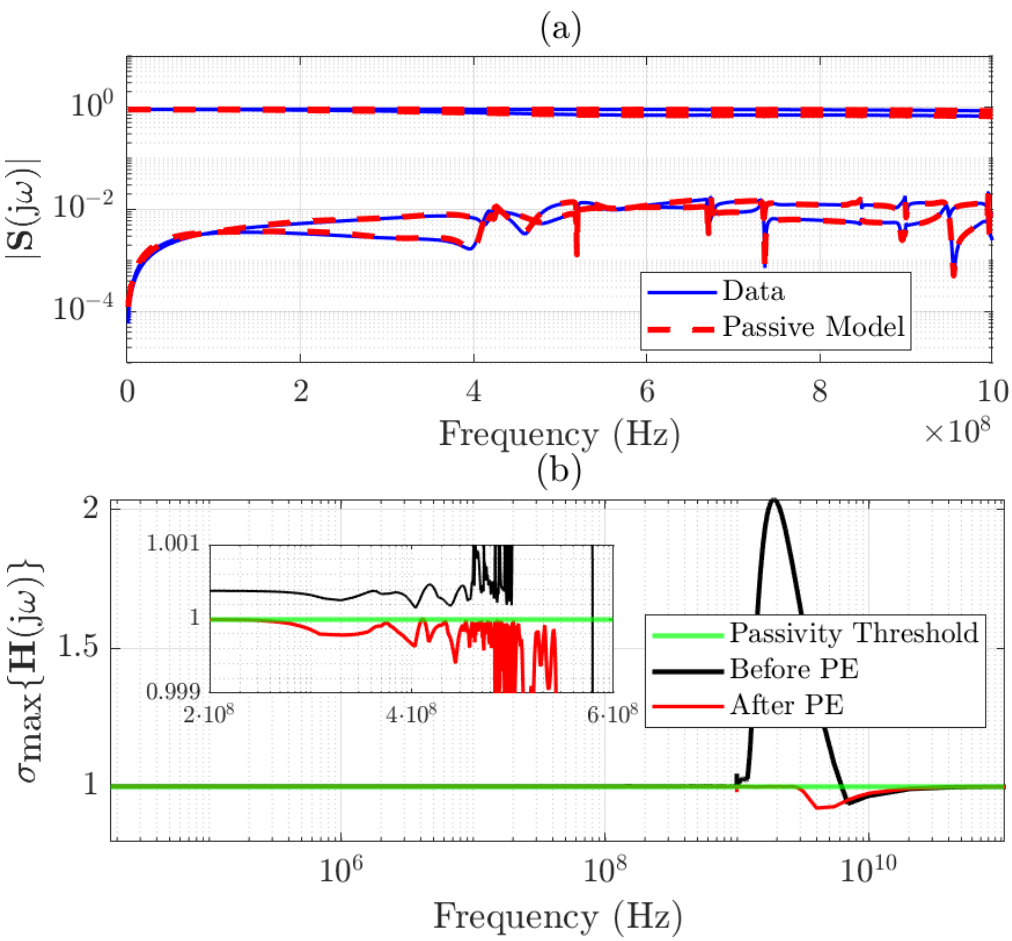


Figure 3. Modelling a 400-port box: (a) model accuracy and (b) maximum singular values after passivity enforcement.

Task 2

The simulation tool based on a modified WR scheme (developed with TUHH) has been tested with systems up to 1024 ports -terminated with 2028 diodes- with a wide range of transient simulations settings. To this end, the WR scheme has been improved with a quasi-Newton solver iteration [28], [29] to speed-up the convergence property of the method, and with a time windowing approach [30] to help us dealing with an increase in the number of variables (i.e., the number of ports and time samples required by the simulation). Results of the proposed method have been compared with HSPICE, the state-of-the-art circuit solver, that allows taking advantage of the macromodel structure (pole-residue transfer function) providing the best configuration to simulate this kind of problems.

The proposed WR scheme provides, under this stressful condition, the same solution of HSPICE with a speed-up factor from 10X to 100X.

Here follow some detail of the investigation, specifically on the comparison with respect to the state-of-the-art simulation tool (SPICE). Results of the proposed WR scheme are also provided.

Accuracy Comparison with SPICE
In this section, the results of the accuracy of the proposed procedure with respect to the state-of-the-art SPICE engine are presented.

Remarks

1. HPSICE automatically selects the integration time-step, while our implementation of the WR scheme relies on a recursive convolution approach that limits us to use a fixed-time step; this limits the comparison of the two methods in terms of accuracy, since any choice to evaluate the discrepancies of the two solutions in terms of errors will be affected by the approximation introduced by the (necessary) interpolation
2. To obtain a fair comparison with respect to HSPICE, we have used an explicit pole-residue model representation in both the WR (MATLAB) and the HSPICE environment; nevertheless, it must be considered that: (a) not all SPICE engines are able to deal with this model representation, that in HSPICE is defined as *FOSTER FORM*; (b) the equivalent circuit representation is less efficient than the explicit pole-residue form (see [31]), and commonly relies on a sparse state-space representation of the model.

The combination of the adaptive time-stepping and the numerical approximations introduced by the change of model synthesis (state-space/pole-residue) can lead to discrepancies in the transient simulation results, even within the SPICE engine framework.

This is confirmed by Figure 4 that shows how two representations of the same model can lead to a different result, even if the same HSPICE engine is used. In the reported case, a 100-port box model has been simulated following [32], with input incident field defined as the derivative of a Gaussian Modulated Pulse centered at 800MHz (amplified with a gain $g = 5$ to exacerbate the nonlinear characteristic of the loads) and terminated on a bridge of diodes. The same model has been simulated with the same simulation settings, but in two different representations: explicitly defining the system in a pole-residue form (Foster, blue lines of Figure 4); synthesizing an equivalent circuit of the model state-space representation (in Fig.4 defined as MNA). Fig.4 clearly shows that the two results are completely different, even if the same HSPICE engine has been used.

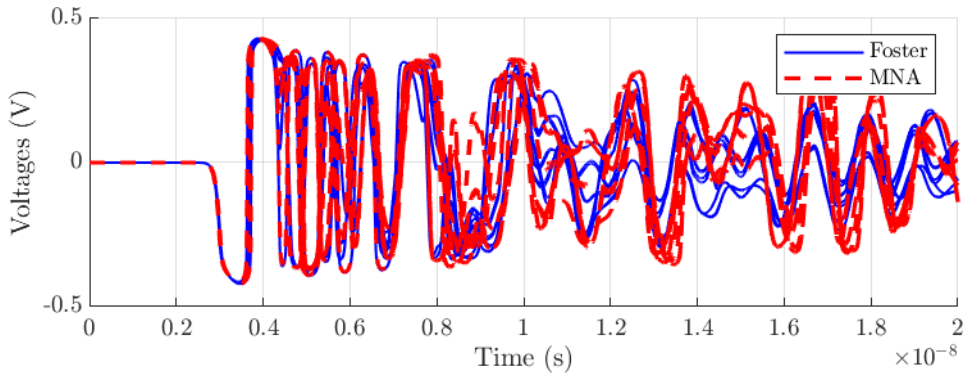


Figure 4. HSPICE results: a 100-port model simulation with explicit pole-residue representation (Foster) and using an equivalent circuit of a state-space representation (MNA).

A more comprehensive example is summarized in Figure 5. In this case, a 400-port box has been excited with the envelop of a Gaussian Modulated Pulse centered at 400MHz, which has been amplified with a gain of $g = 10^4$ to exacerbate the nonlinear characteristic of the loads and further stress the limit of the both simulation engines. Since we have noticed that changing the accuracy threshold of the proposed WR scheme did not improve the final error with respect to the SPICE solution, we have instead systematically increased the accuracy of HSPICE running the same simulation with different setting:

- simulating the model in a state-space representation, synthesized as standard equivalent circuit [31], with default options;
- with default options, and the same model synthesized in an explicit pole-residue form (Foster Form) – case (a) of Fig.5;
- as in case (a) but setting OPTION.ACCURATE = 1 , which allows to boost the SPICE accuracy – case (b) of Fig.5;
- as in case (b) and forcing SPICE to a tight timestep by setting $\mathrm{OPTION.DELMAX} = 10^{-11}$ – case (c) of Fig.5.

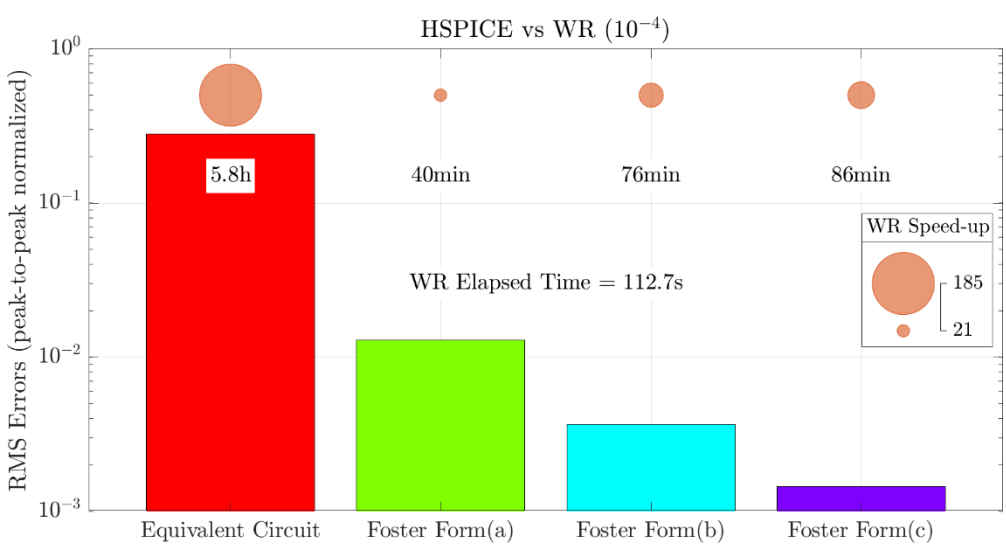


Figure 5. Proposed WR vs SPICE: Simulation results of a 400-port box with different SPICE settings.

Figure 5 clearly shows that improving the SPICE solution leads to the proposed WR result, that is here used as reference to compute the normalized RMS error. Furthermore, the proposed approach provided a relevant speed-up in all cases, ranging from 21X in case of the pole-residue model with standard options to 185X when the model has been simulated in its equivalent circuit representation.

Figure 6 shows a selected response of the simulated 400-port model in pole-residue (Foster) representation with different simulation settings. In particular, the bottom panel shows that when the SPICE accuracy is boosted the Foster solution (blue line) converges to the proposed WR signal (red-dashed line).

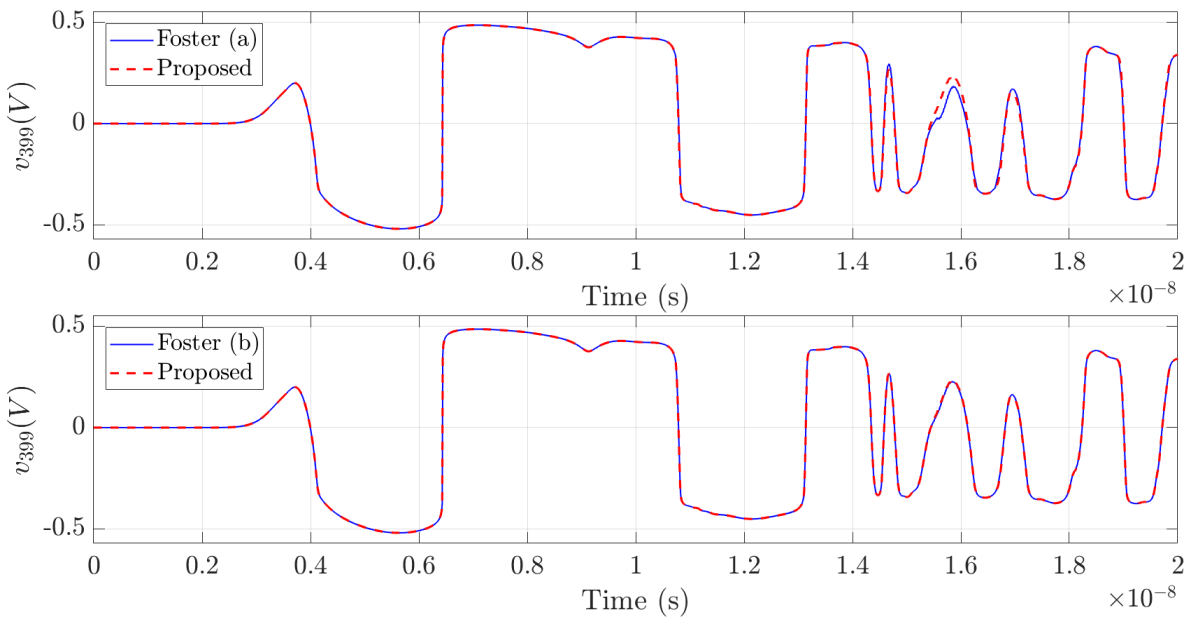


Figure 6. A 400-port example: comparison of the proposed WR scheme with respect to an HSPICE pole-residue model (Foster), run with standard simulation settings (a) and improving HSPICE accuracy (b).

Using the experience from these benchmarks, all presented SPICE results have been generated synthesizing the model in the pole-residues (Foster) form and imposing the accuracy options as in the case (b), with OPTION.ACCURATE flag to 1.

Examples from 100 to 1024 ports

In this section, some simulation examples are reported to further demonstrate the effectiveness of the proposed scheme. In particular, a 100-port and a 1024-port box have been simulated with the same incident field used for the example reported in Figure 5 and 6. Since the selected incident field has been filtered by the open-circuit transfer functions of the two boxes (see [32]), the two simulation settings can be considered as independent, even if the two results will show some similarities.

Figure 7 depicts a set of selected responses of the 100-port model, demonstrating perfect agreement between SPICE and the proposed WR scheme. Indeed, the worst case RMS error computed after interpolation of the SPICE signals is $2.26 \cdot 10^{-3}$.The same level of accuracy (RMS=$1.87 \cdot 10^{-3}$) is reported for the 1024-port case in Figure 8. Both results have been obtained with a major advantage in terms of runtime, as summarized in Table 1, showing a speed-up factor of at least 30X with respect to SPICE.

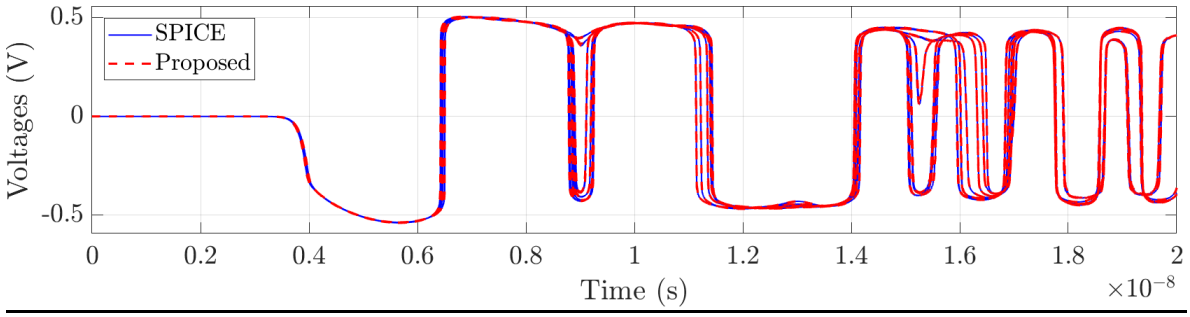


Figure 7. Worst-case RMS error scenario: comparison of the proposed WR scheme with respect to HSPICE for a 100-port box example.

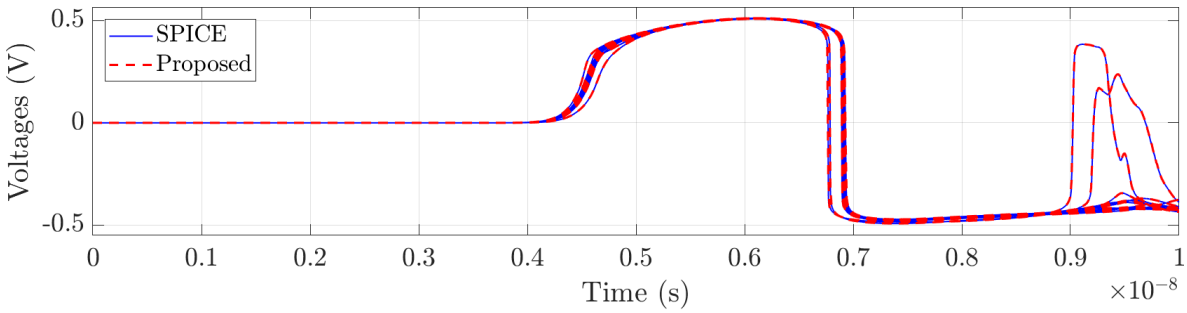


Figure 8. As in Figure 7 for a 1024-port box.

	HSPICE Time	Proposed Time (s)	RMS Error	Speed-Up Factor
100	306.5 sec	8.2	2.26e-03	37.4 X
400	76 min	112.7	3.67e-03	40.5 X
1024	6.4 h	257.8	1.87e-03	89.3 X

Table 1. Summary of results increasing the port size.

Task 3

To address task 3-c of our project and to create a meaningful set of voltage and current time-domain signals of the NL terminations, the exploration of the full nonlinear characteristics of the terminations has been required. To this end, the amplitude of the incident field has been increased, reaching a maximum peak-to-peak excitation voltage greater than 1kV. This setup leads the current state-of-the-art simulation engine close to its limit.

Our tests showed that a ROM of the NL terminations did not improve the simulation performances (task 3-a). The projection of the space of the loads obtained with well-known techniques (as the POD) onto a lower-dimensional subspace did not provide the expected speed-up to the transient simulation: since all ports have been terminated on a diode (or two), the correlation between loads is provided only by the linear system itself.

For this reason, an accurate and compact ROM of the NL terminations can be created only if some of the loads are internally coupled or if each NL load is sufficiently complex (i.e., the states of the NL system are redundant). To obtain these results, a full simulation flow

of the nonlinear terminations has been created and tested, embedding ROM techniques (as the POD) to assess the project feasibility, and including the resulting model in the WR simulation tool (task 3-b).

Here follows the detailed investigation and some example.

MOR on Nonlinear Components: POD & DEIM

We start our investigation defining a simple nonlinear circuitry as it will be used in our WR scheme, depicted in Figure 9. The right hand side of the circuit, consisting of a parallel of a capacitor and an ideal diode, will be the dynamic termination of each port of our box.

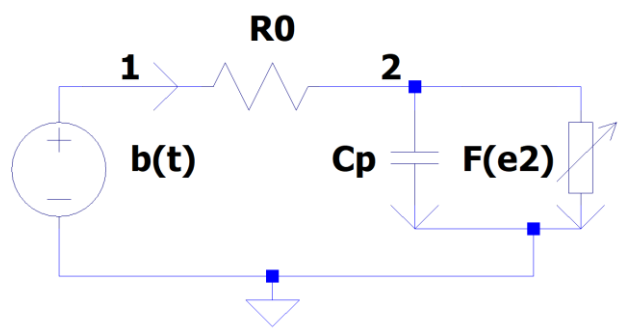


Figure 9. The nonlinear load (parallel of a capacitor and a diode) as solved in the WR scheme. System variables are $\boldsymbol{x}(t) = [e_1\ e_2\ i_1]^T$.

The goals of this investigation are to

1. verify that a ROM of a dynamic nonlinear load can be effectively used for all iterations of the WR scheme;
2. check the efficiency of MOR technique in terms of compression (reduction of the nonlinear number of states).

Our workflow can be summarized in the following steps:

1. Simulate a P-port dynamic nonlinear circuitry in MATLAB (e.g. as in [23])
2. Apply MOR techniques as POD and DEIM
3. Include the dynamic NL load in the WR scheme.

We start from step 1, defining the system equations as in [23]

$$\mathbf{C}\,\frac{d}{dt}\mathbf{x}(t) + \mathbf{F}\big(\mathbf{x}(t)\big) = \mathbf{B}\mathbf{u}(t)$$
$$\mathbf{y}(t) = \mathbf{L}\mathbf{x}(t)$$

where **C**, **G** in $\mathrm{R}^{n\times n}$ collect the stamps of memory and memoryless elements, $\mathbf{x}(\mathrm{t}) \in \mathrm{R}^n$ is a vector of the node-voltage waveforms, currents in inductors and voltage sources, charges in the nonlinear capacitors and magnetic fluxes in nonlinear inductors. $\mathbf{F}(\mathbf{x}(\mathrm{t})) \in \mathrm{R}^n$ is a nonlinear vector that represents the contribution of nonlinear functions (conductances, capacitors and inductors contributions).

We solved the circuit in Figure 9 using MATLAB solvers (ode15i/s), providing the Jacobian of the system and replicating the dynamic load P times to obtain a multiport system.

We then applied the POD scheme as in [23] using a Galerkin projection to obtain a Reduced Order Model (ROM) defined as

$$\hat{\mathbf{C}}\,\frac{d}{dt}\hat{\mathbf{x}}(t) + \hat{\mathbf{F}}\big(\hat{\mathbf{x}}(t)\big) = \hat{\mathbf{B}}\mathbf{u}(t)$$
$$\mathbf{y}(t) = \hat{\mathbf{L}}\hat{\mathbf{x}}(t)$$

where the change of variable $\boldsymbol{x}(t) = V\hat{\boldsymbol{x}}(t)$ is applied to the original system equations.

We recall that the projection matrix $\boldsymbol{V}$ is obtained applying a Singular Value Decomposition to the matrix that collects the evolution of the system states $\mathbf{x}(t)$ at several instants of time. See [23] for details. The above procedure preserves the Jacobian size and does not improve the simulation runtime.

Nevertheless, this first approach provides already a good feasibility test to estimate the impact of advanced MOR techniques - such as DEIM – that will be used to optimized and compress the Jacobian of the ROM.

We then applied the following test:

1. We simulated a 100-port box in SPICE, terminating each port on the parallel of a capacitor and a diode (the dynamic load of Figure 9); this step allows us to obtain
    a. the box scattering waves $\breve{\boldsymbol{a}}(t), \breve{\boldsymbol{b}}(t)$, that are a proxy to the converged result of the WR scheme;
    b. The converged system state variables $\breve{\boldsymbol{x}}(t)$;
2. We trained a ROM model initializing the voltage source of Figure 9 using the reflected wave $\boldsymbol{b}(t)$ obtained from the first iteration of the WR (see [32]);
3. We simulated the ROM model with the "converged" signal $\breve{\boldsymbol{b}}(t)$ and we checked the accuracy on the resulting state variables $\boldsymbol{x}(t)$.

The results of the reconstruction of the state variables is depicted in Figure 10. The POD model shows a good accuracy predicting the SPICE signals (used as proxy of the converged WR signals).

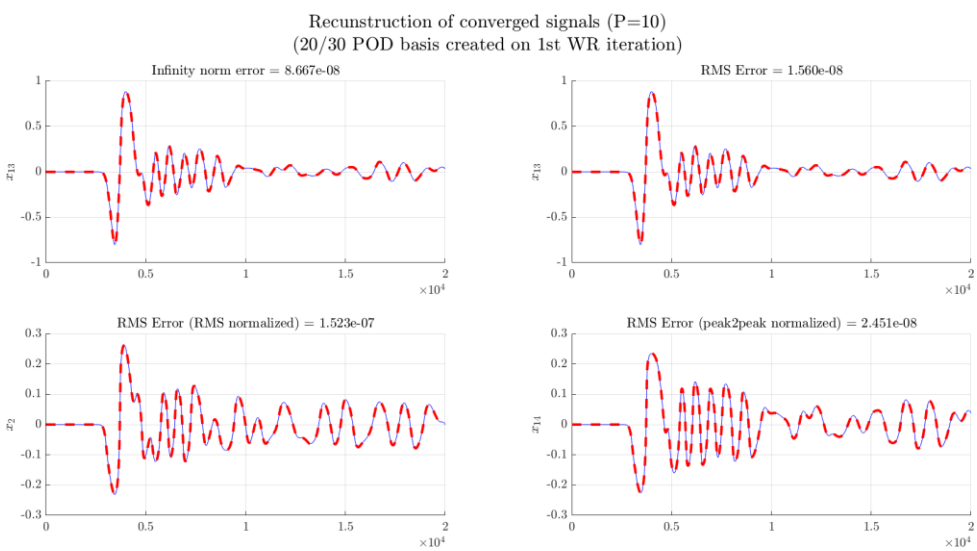
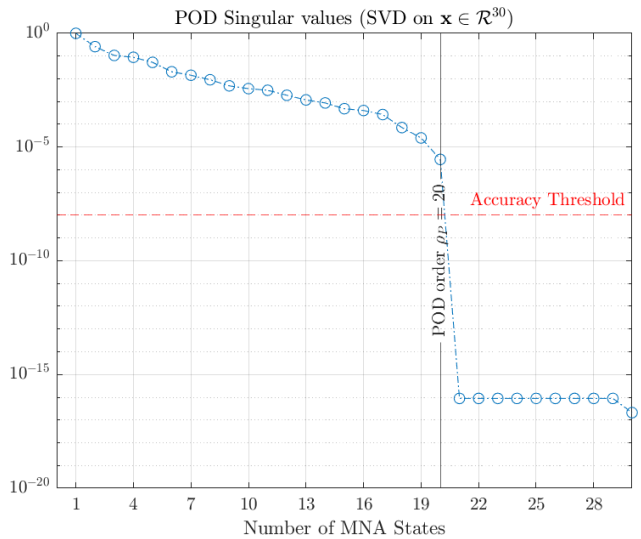


Figure 10. Accuracy of the ROM on SPICE signals, different from the one used to train the model.

Nevertheless, observing the POD singular values, reported in Figure 11, it is clear that the number of retained variable actually corresponds to the minimal number of states (in this case 2, corresponding to i_1 and e_2 of Fig.9) necessary to describe a load replicated P-times. It is now clear that the correlation between loads is provided only by the linear system itself.

The next section will further investigate this aspect, clarifying the simulation set-up.



Simulation Set-up Investigation

In this section, an investigation on the selected simulation set-up is performed. This was not an explicitly task of our project, but it was necessary to verify the correctness of the proposed simulation framework and to justify the results of task-3.

In this investigation we simulated our system using HSPICE changing the loads path to ground, definition two configurations:

a) *each* negative pin of all ports have been connected to ground, as in the left panel of Figure 11
b) only *one* negative pin has been connected to ground, meaning that P-1 ports have been left *floating* (without an explicit DC connection to ground), as in the right panel of Figure 11.

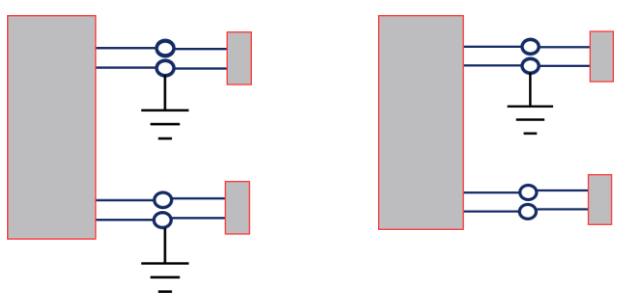


Figure 11. Simulation set-up ground test: are the these two benchmarks equivalent?

Figure 12 shows the results for two boxes, with 9 and 100 ports respectively. Both simulations have been performed connecting ideal diodes to a SPICE synthesis of the model: the 9-box (top panel of Fig.12) has been synthesized as an equivalent circuit of a state-space model representation; the 100-port (bottom panel of Fig.12) has been synthesized in an explicit pole-residue (Foster) form.

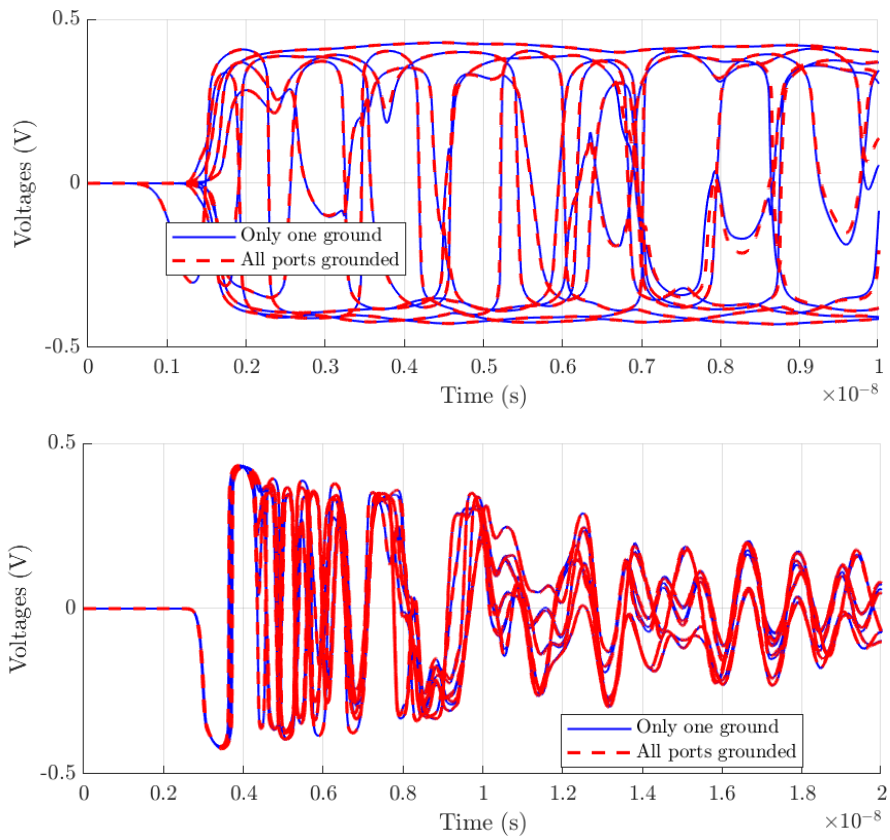


Figure 12. Selected set of responses for a 9-port (top) and a 100-port (bottom) box changing the ground definition (see Fig.11).

On the one hand, it is clear that the two ground definitions of Figure 11 produce a small difference only in the equivalent circuit case. On the other hand, the setting b) provided a major improvement in terms of runtime. Indeed, the configuration a) required 30 and 863 seconds for the 9 port and 100 ports, respectively, while the ground definition b) required only 3 and 163 seconds to obtain (almost) the same result.

Since the two set-up are equivalent, any Model Order Reduction technique will not provide a better sparse/compressed representation of the loads: the problem formulation is already the most efficient, and the NL system states (observing only the termination) cannot show any redundancies.

4. Conclusions

Even if the expected outcomes have not been reached for all tasks, this work provided an improvement in the state-of-the-art of numerical simulation of electrically large

electromagnetic structures terminated on NL loads and mixed with MOR techniques, addressing and successfully completing most of the planned tasks, and resulting in several publications.

Indeed, the collaboration with TUHH resulted in a publication in the IEEE Transactions on Electromagnetic Compatibility, entitled “Iteration Dependent Waveform Relaxation for Hybrid Field Nonlinear Circuit Problems” [33], in a submitted manuscript for the same IEEE Transaction entitled “Regularized and Compressed Large-Scale Rational Macromodeling: Theory and Application to Energy-Selective Shielding Enclosures” [24], and in a manuscript submitted to the SPI 2022 – 26th IEEE Workshop on Signal and Power Integrity, entitled “Low-Frequency Modal Extrapolation and Regularization for Full-Bandwidth Macromodeling of Electromagnetic Structures” [25]. Further achievements are expected in the next future. All above results will be part of my PhD. thesis, “Fast Simulations of Nonlinearly Loaded Large-Scale Systems via Reduced Order Models. A Case Study: Energy Selective Surfaces”, which will be submitted by May 2022.

5. References

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