

# PWR/GND Plane PCB with 11x11 Via-Array

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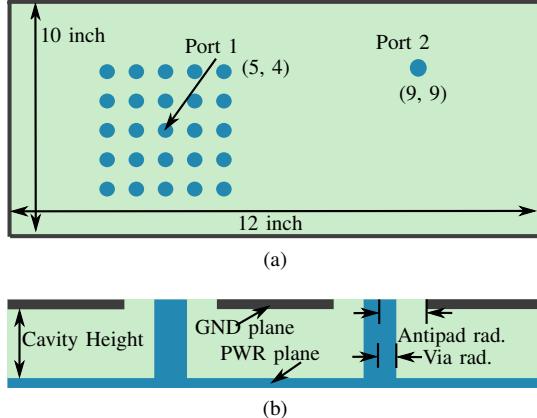


Fig. 1: For clarity the size of the via array is increased and the number of vias is reduced. The center of the via array is the port under investigation. All dimensions are in inch. (a) top view, (b) cross view. Figures adapted from [2].

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## I. DESCRIPTION

This structure consists of a power delivery network (PDN) on a PCB with one cavity, a power plane on the bottom and a ground plane on top, as shown in Fig. 1 (b). A more detailed description is given in [11], [12]. Port 2 is in the center of a via-array and is the port that is decoupled by placing decoupling capacitors (decaps) on the surrounding via array. At this port the impedance of the PDN is observed. With this configuration the impact of decaps on the PDN impedance was investigated. The variations for this structure include changing the distance of the planes, the material properties and the decaps. For the decaps the location, capacitance and number was varied. The capacitors were chosen from a library containing overall 15 values including equivalent series resistance and equivalent series inductance.

## II. MODELING TOOL

All simulations have been carried out with a physics-based (PB) approach [?], [?], [1]. A demo version of the tool can be accessed over [www.tet.tuhh.de](http://www.tet.tuhh.de). All information regarding the setup are described in the following.

## III. PARAMETER

If a value is given in the tables the parameter is not altered during the simulations. On the other hand if the value is varied the according entry of the `<parameter.csv>` file is given.

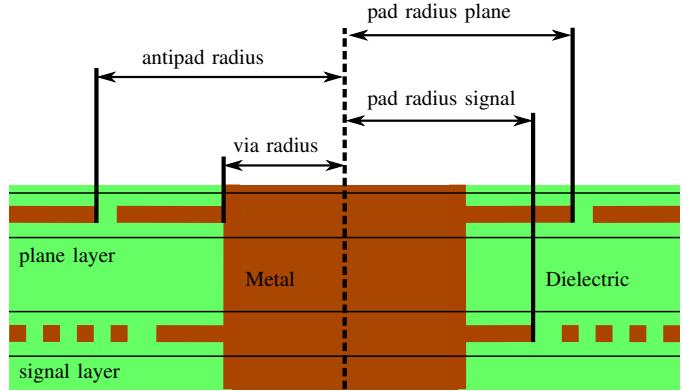


Fig. 2: Via model used for all vias of the structure. If the radius values are not given the `via_radius` is used for `pad_radius_plane`, and `pad_radius_signal`.

### A. Via Model

The dimensions of the vias used in the structure shown in Fig. 1 are given in Fig. 2. All vias are based on this model. For the dielectric material (Dielectric) the rel. permittivity ( $\epsilon_r$ ) and the loss tangent ( $\tan \delta$ ) are given. For the conductive material (Metal) the conductivity ( $\sigma$ ) is given. An overview is given in Tab. I.

Table I: Overview of the parameters used in the via model, as shown in Fig. 2

Parameter	Value
via radius	5 mil
antipad radius	18 mil
pad radius plane	5 mil
pad radius signal	5 mil

### B. Materials

Two different materials were used, the material for the metal e.g. planes, striplines, vias, pads, and the material for the dielectric e.g. cavity filling, antipad. The metal requires two parameter conductivity ( $\sigma$ ) and rel. permeability ( $\mu_r$ ). The dielectric has the rel. permittivity ( $\epsilon_r$ ) and the loss tangent ( $\tan \delta$ ). An overview is given in Tab. II.

### C. Stackup

For the stackup general parameters are introduced. If not stated differently in the description the naming refers to all cavities of the stackup. One cavity is defined by the enclosed dielectric material by two planes, as shown in Fig. 3. Signal

Table II: Overview of the material parameters used in the structure.

Parameter	Value
$\sigma$	conductivity
$\mu_r$	1
$\epsilon_r$	epsilon_r
$\tan \delta$	loss_tangent

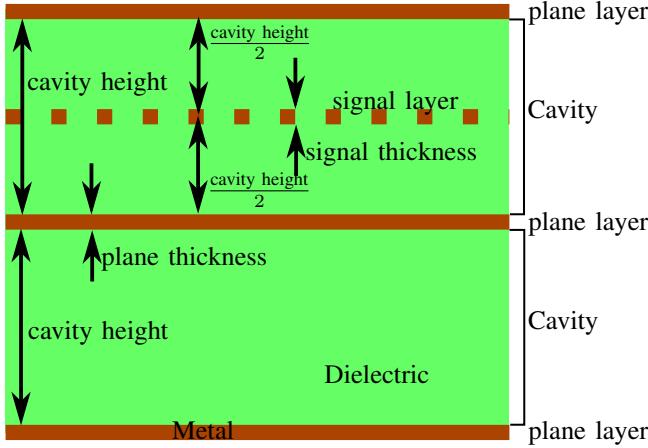


Fig. 3: Stackup nomenclature for the problem. The naming refers to all cavities unless stated differently in the description.

layers are defined in the middle of the cavity. The cavity height is the distance between two plane layers (here diel\_height).

Table III: Overview of the parameters related to the stackup used in the PCB.

Parameter	Value
cavity height	diel_height
plane thickness	1 mil
signal thickness	1 mil

#### D. File *<parameter.csv>*

The file *<parameter.csv>* contains all necessary information for the setup of the geometry and parameter variations. The columns are:

- index
- diel\_height (Cavity Height)
- epsilon\_r
- loss\_tangent
- conductivity
- ic\_x (of Port 2)
- ic\_y (of Port 2)
- simuIndex
- {ESR/ESL/C/xPos/yPos}

Index is the row in the *<parameter.csv>*, diel\_height is the distance between the two metal planes, epsilon\_r is the relative permittivity ( $\epsilon_r$ ) of the dielectric between the power and ground planes, loss\_tangent is  $\tan(\delta)$  of the dielectric, conductivity is the conductivity of the planes and the via

material, [ic\_x and ic\_y] is the center of the via-array, simuIndex is the simulation index (<index>) to find the simulation results. The last column ({ESR/ESL/C/xPos/yPos}) is a list of the placed capacitors. For each capacitor the equivalent series resistance (ESR), equivalent series inductance (ESL), capacitance (C), absolute x position on the PCB and absolute y position on the PCB is given. As delimiter "/" (slash) is chosen.

#### IV. PUBLICATIONS

This structure was used in [2], [3]. In both publications investigations with respect to machine learning (ML) techniques were made.

#### REFERENCES

- [1] R. Rimolo-Donadio, X. Gu, Y. Kwark, M. Ritter, B. Archambeault, F. de Paulis, Y. Zhang, J. Fan, H.-D. Brüns, and C. Schuster, "Physics-Based Via and Trace Models for Efficient Link Simulation on Multilayer Structures Up to 40 GHz," *IEEE Transactions Microwave Theory and Techniques*, vol. 57, no. 8, pp. 2072–2083, Aug. 2009.
- [2] C. M. Schierholz, K. Scharff, and C. Schuster, "Evaluation of Neural Networks to Predict Target Impedance Violations of Power Delivery Networks," in *IEEE 28th Conf. Electrical Performance Electronic Packaging and Systems EPEPS*, Montreal, CA, Oct. 2019.
- [3] M. Schierholz, C. Yang, K. Roy, M. Swaminathan, and C. Schuster, "Comparison of Collaborative versus Extended Artificial Neural Networks for PDN Design." IEEE, May 2020. [Online]. Available: <https://doi.org/10.1109/spi48784.2020.9218157>